User Manual

8550/8551

50 MHz
Modulated Function/Pulse Generators

Tabor Electronics Ltd.

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WARRANTY

Tabor warrants that all products manufactured by Tabor conform to published Tabor specifications and are free from defects in material and workmanship for a period of one (1) year from the date of delivery when used under normal conditions and within the service conditions for which they were furnished.

The obligation of Tabor arising from a Warranty claim shall be limited to repairing, or at its option, replacing without charge, any product which in Tabor's sole opinion proves to be defective within the scope of the Warranty. In the event Tabor is not able to modify, repair or replace non-conforming defective parts or components to the condition as warranted within a reasonable time after receipt thereof, Buyers shall be credited for their value at the original purchase price.

Tabor must be notified in writing of the defect or nonconformity within the Warranty period and the affected product returned to Tabor's factory or to an authorized service center within thirty (30) days after discovery of such defect or nonconformity.

For products warranties requiring return to Tabor, products must be returned to a service facility designated by Tabor. Buyer shall prepay shipping charges, taxes, duties and insurance for products returned to Tabor for warranty service. Except for products returned to Buyer from another country, Tabor shall pay for return of product to Buyer.

Tabor shall have no responsibility hereunder for any defect or damage caused by improper storage, improper installation, unauthorized modification, misuse, neglect, inadequate maintenance, accident or for any product which has been repaired or altered by anyone other than Tabor or its authorized representative and not in accordance with instructions furnished by Tabor.

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Tabor Electronics Ltd.

REPAIR AND CALIBRATION REQUEST FORM

To allow us to better understand your repair requests, we suggest you use the following outline when calling and include a copy with your instrument to be sent to the Tabor Repair Facility.

Model_____ Serial No._____ Date_____

Company Name_____ Purchase Order #_____

Billing Address_____
City

State/Province Zip/Postal Code Country

Shipping Address_____
City

State/Province Zip/Postal Code Country

Technical Contact_____ Phone Number ( )_____
Purchasing Contact _____ Phone Number ( )_____

1. Describe, in detail, the problem and symptoms you are having. Please include all set up details, such as input/output levels, frequencies, waveform details, etc.

2. If problem is occurring when unit is in remote, please list the program strings used and the controller type.

3. Please give any additional information you feel would be beneficial in facilitating a faster repair time (i.e., modifications, etc.)

4. Is calibration data required? Yes No (please circle one)

Call before shipping
Note: We do not accept "collect" shipments.

Ship instruments to nearest support office listed on back.

SAFETY PRECAUTIONS

Protect yourself. Follow these precautions:

- Don’t bypass the power cord’s ground lead with two-wire extension cords or plug adapters.
- Don’t disconnect the green and yellow safety-earth-ground wire that connects the ground lug of the power receptacle to the chassis ground terminal (marked with or
- Don’t plug in the power cord until directed to by the installation instructions.
- Don’t repair the instrument unless you are qualified electronics technician and know how to work with hazardous voltages.
- Pay attention to the **WARNING** statements. They point out situations that can cause injury or death.
- Pay attention to the **CAUTION** statements. They point out situations that can cause equipment damage.

The American National Standard Institute (ANSI) states that a shock hazard exists when voltage levels greater than 30V RMS, 42.4V peak, or 60 VDC are present. A good safety practice is to expect that hazardous voltage is present in any unknown circuit before touching or disconnecting the line cord. Before operating this instrument, make sure the line cord is connected to a properly grounded power receptacle. Inspect the connecting cables and test leads for possible wear, cracks, or breaks before each use.

For maximum safety, do not touch the product, test cables, or any other of the instrument parts while power is applied to the circuit under test. **ALWAYS** remove power from the entire test system before connecting cables or jumpers, or making internal changes. Do not touch any object that could provide a current path to the common side of the circuit under test or power line (earth) ground. Always keep dry hands while handling the instrument. If you are using test fixtures, keep the lid closed while power is applied to the device under test. Safe operation requires that the instrument covers be closed at all times during operation.

Carefully read the Safety Precautions instructions that are supplied with your instrument. Instruments, cables, leads or cords should not be connected to humans. Before performing any maintenance, disconnect the line cord and all test cables.

DECLARATION OF CONFORMITY

We: Tabor Electronics Ltd.
9 Hatasia Street, Tel Hanan
ISRAEL 20302

declare, that the 50 MHz Pulse/Function Generators

Model 8550 and Model 8551

meet the intent of Directive 89/336/EEC for Electromagnetic Compatibility and complies with the requirements of the Low Voltage Directive 73/23/EEC. Compliance was demonstrated to the following specifications as listed in the official Journal of the European Communities:

Safety:
EN 61010-1
IEC 1010-1 (1990) + Amendment 1 (1992)

EMC:
EN 50081-1 Emissions:
EN 55022 - Radiated, Class B
EN 55022 - Conducted, Class B
EN 50082-1 Immunity:
IEC 801-2 (1991) - Electrostatic Discharge
IEC 801-3 / ENV50140 (1993) - RF Radiated
IEC 801-4 (1991) - Fast Transients

Model 8550 and Model 8551 were tested in typical configuration.

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1-1. INTRODUCTION

This manual provides operation and maintenance information for both Model 8550 - Function Generator and Model 8551 - Pulse/Function Generator. Section 1 provides general description of the instruments. Sections 2 and 3 contain installation and operation instructions. IEEE-488.2 (GPIB) programming is explained in Section 4. Maintenance and performance checks are provided in section 5. Theory of operation is described in section 6. Section 7 outlines calibration and troubleshooting procedure. Section 8 contain tables of replaceable parts and recommended spare parts. Section 9 contains schematic and component location diagrams.

NOTE

This manual is common to both Model 8550 and Model 8551. It describes all features and functions for both models. Therefore, some features which are described in this manual may not be available in your instrument. Features that are unique to the Model 8551 are described separately.

1-2. DESCRIPTION

Model 8550 is an extremely high-performance programmable function generator. It provides a variety of signal waveforms, to be used as test stimuli for different electronic devices. Microprocessor based, Model 8550 is easy to set up for manual use. It is also simple to program in GPIB system environment.

The instrument is built in an all-round metal case for improved RFI and EMI shielding. It is housed in a size to fit half-rack enclosures. Regardless of its small size, Model 8550 offers many features and functions, such as enhanced accuracy, eight different linear and logarithmic sweep modes, automatic phase lock loop, pulse and ramp waveforms with transition time control (Model 8551 only), counted burst, internal trigger generator, full implementation of the new IEEE-488.2 standard, and more. But, most of all, Model 8550 guarantees high quality waveforms throughout the specified frequency range, amplitude span, and operating temperature.

Model 8550 generates waveforms within a frequency range from 10mHz to 50MHz and an amplitude span from 10mV to 32Vp-p. Such broad coverage warrants a variety of complex applications. Rapid, repeatable testing every time is assured by a non-volatile memory. Up to 30 front panel set-ups can be stored and recalled for later use; ensuring exact duplication of previous tests. Its performance, programmability and economy make it equally at home in every laboratory.

For improved output accuracy, Model 8550 employs a built-in counter. This counter is incorporated in an internal loop which constantly monitors the output frequency. Even the slightest deviation from the programmed frequency is detected and corrected by the microprocessor circuit.

Model 8550 features self-calibration and self-diagnostic functions that can be operated anytime from the front panel or GPIB command. The self-calibration function compares the output signal parameters to built-in internal references and stores correcting factors in special tables. If calibration routine fails or can not be completed due to electrical faults, the generator produces a failure list that can be evaluated either from the front panel or through GPIB status reporting command.

Besides its normal continuous mode, Model 8550 offers a variety of interrupted and controlled modes. Output waveform may be gated, triggered, or may generate a counted burst of output waveforms. A built-in trigger generator, having a programmable

period, can replace an external trigger stimulant. The MANUAL trigger is just an additional convenience for front panel operation. The generator may also be placed in a number of externally controlled modes, such as VCO, FM, AM, and pulse width modulation (PWM - Model 8551 only).

Model 8550 may be used as an independent sweep generator with its output swept over an exceptionally wide range of 10 decades. The instrument offers a choice of eight sweep modes, both linear and logarithmic to cover a large number of applications. A MARKER output provides an oscilloscope Z-axis modulation to intensify segments of sweep trace.

Alternately, Model 8550 may also be used as a stand-alone phase lock generator. The instrument locks automatically to an external signal and equates its output frequency and phase to that provided by the external reference. The operator may then generate a phase offset between the reference signal and the generator's output. Phase offset is adjusted within a range of ±180°.

Model 8550 provides an output level from 20mV to 32Vp-p into open circuit or 10mV to 16Vp-p into 50Ω. DC offset plus amplitude are independently variable within two window levels: ±16V and ±1.6V (into open circuit). This special characteristics warrants production of extremely small signals at an elevated DC environment.

Model 8551 is a pulse/function generator and is also described in this manual. This instrument is identical in its basic functions to the Model 8550. In addition, this instrument offers Pulse and Ramp waveforms. Pulse width and ramp width are adjustable within a range of 10.0ns to 999ms.

Model 8551 provides control over the transition times for the leading and trailing edges; each can be adjusted independently within a common range. Pulse complement and inverted ramp functions are also available. This manual identifies those features and specifications that only apply to Model 8551.

1-3. INSTRUMENT & MANUAL IDENTIFICATION

The serial number of the instrument is located on the rear panel of the instrument. The two most significant digits identify instrument modifications. If this prefix differs from that listed on the title page of this manual, there are differences between this manual and your instrument.

Technical corrections to this manual (if any) are listed in the back of this manual on an enclosed MANUAL CHANGES sheet.

1-4. OPTIONS

Model 8550 offers a rack mounting option; designated as OPT 001. Opt 001 is field installable or may be ordered with new instruments from the factory.

1-5. SAFETY CONSIDERATIONS

Model 8550 has been manufactured according to international safety standards. The instrument meets EN 61010-1 and UL 1244 standards for safety of commercial electronic measuring and test equipment for instruments with an exposed metal chassis that is directly connected to earth via the power supply cable. Before the instrument is switched on, make sure that protective earth terminal is connected to a protective earth via the power cord. Do not remove instrument covers when operating or when power cord is connected to mains.

Any adjustment, maintenance and repair of the opened instrument under voltage should be avoided as much as possible, but when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

1-6. ACCESSORIES SUPPLIED

Model 8550 is supplied with ac power cord and with an instruction manual. Extra manual is available on request.

1-7. SPECIFICATIONS

Instrument specifications are listed in Tables 1-1. These specifications are the performance standards or limits against which the instrument is tested.

NOTE

All specifications in the following table apply under the following conditions: main signal output terminated into 50Ω, within ±5°C and 24 hours of last internal calibration, and after 30 minutes of warm-up time within a temperature range of 0 to 50°C.

Table 1-1. Model 8550/8551 Specifications

WAVEFORMS:	Sine, Triangle, Square, Positive Pulse, Negative Pulse, Ramp (Model 8551), DC (Model 8550)

FREQUENCY CHARACTERISTICS

Range:	10.00mHz to 50.00MHz.
Resolution:	4 digits
Accuracy:	
Continuous Mode:	±3% of reading, from 10mHz to 999.9mHz; ±0.1%, from 1.000Hz to 50.00MHz;
VCO, and Interrupted Modes:	±3% of reading, to 50.00MHz.
Jitter:	<0.1% ±50ps.

WAVEFORM CHARACTERISTICS

Sine Wave	
Total Harmonic Distortion:	<1%, from 10.00mHz to 100.0KHz.
Harmonic signals below the carrier level:	>40dB, 100KHz - 2.000MHz; >21dB, 2.000MHz - 50.00MHz.
Flatness:	±1%, 10.00mHz to 999.9KHz; ±2%, 1.000MHz to 9.999MHz; −15%, 10.00MHz to 50.00MHz.
Triangle	
Linearity (10% to 90% of amplitude):	<1%, 10.00mHz to 5.000MHz; <3%, 5.000MHz to 20.00MHz; <8%, 20.00MHz to 50.00MHz;
Flatness:	±3%, 10.00mHz to 999.9KHz; ±5%, 1.000MHz to 9.999MHz; −25%, 10.00MHz to 50.00MHz.
Square Wave, Pulse:	
Rise/Fall time:	<6ns, 10% to 90% of amplitude (5 ns typical).
Aberration:	<5%.
SYNC Pulse:	
Output Level:	0 to 1V, into 50Ω; 0 to 2V, open circuit.
Rise/Fall time:	<3ns, into 50Ω.
Aberrations:	<5%.

OUTPUT CHARACTERISTICS

Output Stand-by:	Output Normal or Disabled.
Impedance:	50Ω, ±1%.
Output Level:	20.0mV to 32.0Vp-p, into open circuit; 10.0mV to 16.0Vp-p, into 50Ω.
Resolution:	3 digits.
Accuracy (1 KHz):	±4% of reading, from 10.0mV to 16.0V.

Table 1-1. Model 8550/8551 Specifications (continued)

Level Windows:	±800mV, for amplitude from 10.0mV to 99.9mV; ±8V, for amplitude from 100mV to 16.0V.
Output Protection:	Protected against continuous short to case ground.
Offset	
Resolution:	3 digits
Range:	Offset and amplitude are independently adjustable within level windows of ±800mV and ±8.00V.
Within ±800mV	0 to ±795mV;
Within ±8V	0 to ±7.95V.
Accuracy:	±(1% of setting + 1% of amplitude + .2mV), within ±800mV; ±(1% of setting + 1% of amplitude + 2mV), within ±8V.

DC CHARACTERISTICS (Model 8550 only)

Range:	Variable from −16.0V to +16.0V, into open circuit; −8.00V to +8.00V, into 50Ω.
Resolution:	3 digits with exponent.
Accuracy:	±(1% of reading + 100μV)

TRIGGERING CHARACTERISTICS

Trigger Input:	Via TRIG/REF BNC terminal.
Impedance:	10KΩ, ±5%.
Sensitivity:	500mVp-p.
Max Input Voltage:	±20V
Min Pulsewidth:	20ns.
Slope:	Positive going leading edge
Source:	Manual (front panel push button), internal, or external stimulant.
Modes	
Normal:	Continuous waveform is generated.
Triggered:	Each input cycle generates a single output cycle.
Internal Trigger:	An internal timer repeatedly generates a single output cycle
Gated:	External signal enables generator. First output cycle synchronous with the active slope of the triggering signal. Last cycle of output waveform always completed.
Burst::	Preset number of cycles (1-4000) stimulated by an internal, external, or manual trigger.
Internal Burst:	An internal timer repeatedly generates a burst of counted output cycles
Trigger Frequency:	
External:	To 50MHz.
Internal:	From 20μs to 999s;
Manual:	Simulates an external trigger signal.
Start Phase:	
Offset:	Adjustable, from −90° to +90°, to 500.0KHz; proportionally reduced from 500.1KHz to 50.00MHz..
Accuracy:	±3°, to 500.0KHz
Trigger Level:	variable, −10.0V to +10.0V.

Table 1-1. Model 8550/8551 Specifications (continued)

LOGARITHMIC SWEEP CHARACTERISTICS

Modes:	Auto, Triggered, Gated and Burst. Output frequency repeatedly changes from start sweep to stop sweep settings. Available sweep directions are: up, down, up-down and down-up.
Width:	10 decades maximum.
Rate per Decade:	Continuously adjustable from 10mS to 999S, NOMINAL, per decade.
Steps per decade:	Depends on sweep time and range. Automatically adjusted for maximum steps per sweep time. Maximum steps are 200; minimum steps are 50.
Sweep Output:	1V/decade, below 5 decades; .5V/decade, above 5 decades.
Marker Output:	+5V with no marker; drops to 0V, NOMINAL, when marker frequency is reached and remains at this level until end of sweep.
Stop Sweep Resolution:	Same as Frequency resolution.

LINEAR SWEEP CHARACTERISTICS

Modes:	Same as in logarithmic sweep.
Width:	3 decades maximum.
Time:	Continuously adjustable from 10mS to 999S, NOMINAL.
Sweep Out:	0 to 5V, ±5%.
Sweep Steps:	Depends on sweep time and range. Automatically adjusted by the instrument to get the maximum steps per sweep time. Maximum steps are 1000; minimum steps are 2.
Marker Output:	Same as in logarithmic sweep.
Stop Sweep Resolution:	Same as Frequency resolution.

CONTROL CHARACTERISTICS

Modes:	VCO, AM, FM (Model 8550), PWM (Model 8551)
Input:	Via front panel CONTROL INPUT BNC connector.
Impedance:	10KΩ, ±5%.
Max Input Voltage:	±10V.

VOLTAGE CONTROLLED OSCILLATOR (VCO)/FM CHARACTERISTICS

VCO Sensitivity:	0V to −4.7V, ±20% produces 1/1000 frequency change from main frequency when main frequency is set to 9999 counts.
FM Sensitivity:	0V to 0.5V ±70mV, modulates to 1% deviation from center frequency.
Modulation Bandwidth:	DC to 50KHz.

AM CHARACTERISTICS

Modulation Input:	DC coupled.
Modulation Bandwidth:	DC to 1MHz.
Modulation Range:	0 to 200%; reduced to 70% at 1MHz.
Sensitivity	0V to 5Vp-p produces 100% modulations; 0V to 10Vp-p produces suppressed carrier amplitude modulation (SCAM).

Table 1-1. Model 8550/8551 Specifications (continued)

Envelop Distortion:	<1% for modulation depth <90%, carrier frequency <1.00MHz, and modulation frequency <50KHz; <3% for modulation depth <50%, carrier frequency <50.00MHz, and modulation frequency <50KHz

PHASE LOCK CHARACTERISTICS

Reference Input:	Via TRIG/REF BNC terminal.
Impedance:	10KΩ, ±5%.
Sensitivity:	500mVp-p.
Max Input Voltage:	±20V (dc+peak ac)
Min Pulsewidth:	10ns.
Operation:	Output locks automatically to the frequency and phase of an external signal.
Locking Range:	10Hz to over 60MHz.
Phase Offset	
Range:	Continuously adjustable from –180° to +180°, 10Hz to 19.99MHz.
Resolution:	1°
Accuracy:	±(3° +3% of reading), 10Hz to 100KHz.

PWM CHARACTERISTICS

Sensitivity:	0 to 5V, ±20% produces >10% pulse width change from pulse width setting.
Band Width:	DC to 70KHz.

PULSE/RAMP CHARACTERISTICS (Model 8551 only)

Pulse Modes:	Symmetrical Pulse, Positive Pulse, Negative Pulse and Complement.
Pulse Period	
Range:	20.00ns to 99.99s.
Resolution:	4 digits.
Accuracy and Jitter:	Same as for frequency.
Pulse Width	
Range:	10.0ns to 999ms
Setting Accuracy:	±(5%+2ns), 10.0ns to 99.9ns; ±(4%+2ns), 100ns to 999ms.
Duty Cycle Range:	1% to 8550%, up to 99% using complement mode.
Resolution:	3 digits.
Ramp Modes:	Positive or Negative going ramps.
Ramp Period	
Range:	7.000µs to 99.99s.
Resolution:	4 digits
Ramp Width	
Range:	5.00µs to 999ms.
Setting Accuracy:	3%, 5.00µs to 999ms.
Resolution:	3 digits.
Duty Cycle Range:	1% to 8550%.

Table 1-1. Model 8550/8551 Specifications (continued)

LEAD/TRAIL TIME CONTROL (Model 8551 only)

Range:	8ns to 99.9ms (10% to 90% of amplitude), in 6 overlapping ranges. Leading and trailing edges may be independently programmed within a common range.
In-Range Span:	125:1.
Resolution:	3 digits of programmed value when both transitions are in the first 10:1 portion of their transition time range, decreasing to 2 digits at 100:1.
Accuracy:	±(5% + 2ns), to 99ns; ±(4%+2ns), above 99ns.
Linearity:	3% for transitions >100ns.

GPIB INTERFACE (IEEE-488.2)

Interface Functions:	Complies with IEEE488.2, including queries and common commands.
Programmable controls:	All front panel controls except POWER switch.
Subsets:	SH1, AH1, T6, TE0, L4, LE0, SR1, RL1, PP2, DC1, DT1, C0.
Program Message Format:	Program Message Header, Program Data (floating point and/or suffix program data), Program Message Terminator. Characters lower or upper case.
Response Message Format:	Variable length response format consisting of Response Header, Response Data (NR1, NR2, or NR3 format), and Response Message Terminator.
Common Commands and Queries:	*CAL?, *CLS, *ESE, *ESE?, *ESR, *IDN?, *OPC, *OPC?, *RCL, *RST, *SAV, *SRE, *SRE?, *STB, *TRG, *TST?, *WAI.
Status Reporting:	*ESR?, *STB?, and RQS - read by Serial Poll.
String Termination:	Selectable NL, END (EOI) or combination of both.
Address Selection:	Front panel programming. Address stored in a non-volatile memory.

GENERAL

Display:	4 digits, 7 segment LED's 0.5" high.
Power:	115/230Vac (Optional 100V available), 50 to 400Hz, 100VA max.
Stored Set-ups:	Stores 30 complete sets of front panel set-ups.
Dimensions:	3.5" x 8.3" x 15.4" (H x W x L).
Rack Mount Dimensions:	3.5" x 19" (H x W).
Weight:	Approximately 12Lbs.
Operating Temperature:	0° to 50° C.
Specified Accuracy:	Within ±5° C and 24 hours of last internal calibration.
Storage Temperature:	–40° C to +70° C.
Humidity range:	8550% R.H.
Safety Designed to:	MIL-T-28800D, EN61010, IEC1010-1, UL-1224.
EMC:	EN50081-1, EN55022, EN50082-1, IEC801-2, IEC801-3, IEC801-4.
Vibration:	Operates at a vibration level of 0.013 in. from 5 to 55Hz (2g at 55Hz)
Shock:	Non-operating, 40g 9ms half-sine pulse.

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Preparation Section 2

2-1. INTRODUCTION

This section contains information and instructions necessary for the installation and shipping of the Model 8550 and Model 8551. Details are provided for initial inspection, voltage selection, primary power frequency, power connection, grounding safety requirements, installation information, and re-packing instructions for storage or shipment.

2-2. UNPACKING AND INITIAL INSPECTION

Unpacking and handling of the counter requires only the normal precautions and procedures applicable to the handling of sensitive electronic equipment. The contents of all shipping containers should be checked for included accessories and certified against the packing slip to ascertain that the shipment is complete.

2-3. PERFORMANCE CHECKS

The instrument was carefully inspected for mechanical and electrical performance before shipment from the factory. It should be free of physical defects and in perfect electrical order upon receipt. Check the instrument for damage in transit and perform the electrical procedures outlined in Section 5. If there is indication of damage or deficiency, see the warranty in this manual and notify your local Tabor field engineering representative or the factory.

CAUTION

It is recommended that the operator be fully familiar with the specifications and all sections of this manual. Failure to do so may compromise the warranty and the accuracy which Tabor has engineered into your instrument.

2-4. LINE VOLTAGE AND FUSES

The Model 8550 accepts a primary input voltage from one of the following sources: a. 103.5 to 126.5 Vac (115 Vac, NOMINAL) b. 207 to 253 Vac (230 Vac, NOMINAL) Tabor ships the Model 8550 set for the line voltage and with the proper fuse for the destination country. Figure 2-1 illustrates the location of the line voltage switch and fuse holeder.

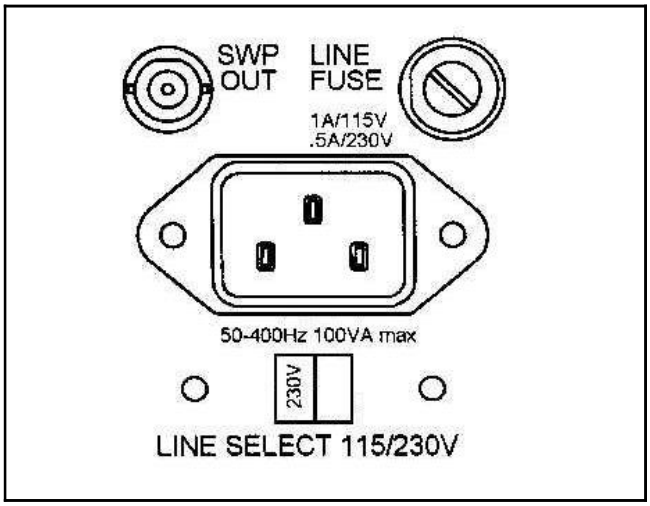

Figure 2-1. Line Voltage and Fuse Holder.

The instrument operates over the power mains frequency range of 50 to 400Hz. Always verify that the operating power mains voltage is the same as that specified on the rear panel voltage selector switch.

CAUTION

Failure to switch the instrument to match the operating line voltage will damage the instrument and may void the warranty.

The Model 8550 should be operated from a power source with its neutral at or near ground (earth potential). The instrument is not intended for operation from two phases of a multiphase ac system or across the legs of a single-phase, three-wire ac power system. Crest factor (ratio of peak voltage to rms) should be typically within the range of 1.3 to 1.6 at 10% of the nominal rms mains voltage.

To change the line voltage, disconnect the power cord from the Model 8550, slide the Line Select switch (Figure 2-1) to the desired line voltage. Also be sure to change the fuse; see the following procedure.

To change the fuse, perform the following steps:

1. Disconnect the power cord from the instrument. Remove the fuse from the fuse holder.

2. Compare the ampere rating on the fuse to the ampere ratings given in Table 2-1. If the fuse is blown, replace it by sliding the new fuse back into the fuse holder. If the fuse is not blown and has the right rating, keep it. If the fuse has the wrong rating, replace the new fuse into the fuse holder.

3. Connect the ac line cord to the power connector at the rear of the unit and the power source.

AC Voltage	Selection	Fuse
103.5 to 126.5	115	1 amp, slo-blo
207.0 to 253.0	230	0.5 amp, slo-blo

Table 2-1. Line Voltage and Fuse Selection.

2-5. GROUNDING REQUIREMENTS

To insure the safety of operating personnel, the U.S. O.S.H.A. (Occupational Safety and Health) requirement and good engineering practice mandate that the instrument panel and enclosure be “earth” grounded. All of Tabor instruments are provided with an Underwriters Laboratories (U.L. and V.D.E) listed three-conductor power cable, which when plugged into an appropriate power receptacle, grounds the instrument. The long offset pin on the male end of the power cable carries the ground wire to the long pin of the Euro connector (DIN standard) receptacle on the rear panel of the instrument.

To preserve the safety protection feature when operating the instrument from a two-contact outlet, use a three-prong to two-prong adapter and connect the green lead on the adapter to an “earth” ground.

CAUTION

To avoid operator shock hazard do not exceed the power mains voltage frequency rating which limits the leakage current between case and power mains. Never expose the instrument to rain, excessive moisture, or condensation.

2-6. INSTALLATION AND MOUNTING

The instrument is fully solid state and dissipates only a small amount of power. No special cooling is required. However, the instrument should not be operated where the ambient temperature exceeds 40° C, when the relative humidity exceeds 8550% or condensation appears anywhere on the instrument. Avoid operating the instrument close to strong magnetic fields which may be found near high power equipment such as motors, pumps, solenoids, or high power cables. Use care when rack mounting to locate the instrument away from sources of excessive heat or magnetic fields. Always leave 4 cm (1.5 inches) of ventilation space on all sides of the instrument.

2-7. BENCH OPERATION

The Model 8550/8551 is shipped with plastic feet, tilt stand in place and ready for use as a bench or portable instrument. See outline drawing Figure 2-1 for dimensions.

2-8. RACK MOUNTING

The instrument may be rack mounted in a standard 19 inch rack. The instrument may be rack mounted in Rack Mount Kit option 001.

2-9. PORTABLE USE

The instrument may be used in applications requiring portability. A tilt stand consisting of two retractable legs is provided with each unit.

2-10. SHORT TERM STORAGE

If the instrument is to be stored for a short period of time (less than three months), place cardboard over the panel and cover the instrument with suitable protective covering such as a plastic bag or strong craft paper. Place power cable and other accessories with the instrument. Store the covered voltmeter in a clean dry area that is not subject to extreme temperature variations or conditions which may cause moisture to condense on the instrument.

2-11. LONG TERM STORAGE OR RE-PACKAGING FOR SHIPMENT

If the instrument is to be stored for a long period or shipped, proceed as directed below. If you have any questions contact your local Tabor field engineering representative or the Tabor Service Department at the factory.

If the original Tabor supplied packaging is to be used proceed as follows:

1. If the original wrappings, packing material, and container have been saved, re-pack the instrument and accessories originally shipped to you. If the original container is not available, one may be purchased through the Tabor Service Department at the factory.

2. Be sure the carton is well sealed with strong tape or metal straps.

3. Mark the carton with the model number and serial number with indelible marking. If it is to be shipped, show sending address and return address on two sides of the box; cover all previous shipping labels.

If the original container is not available, proceed as follows:

1. Before packing the unit, place all accessories into a plastic bag and seal the bag.

2. For extended storage or long distance shipping only, use U.S. government packing method II C and tape a two-unit bag of desiccant (per MIL-D-3464) on the rear cover.

3. Place a 13 cm (5 inch) by 30 cm (12 inch) piece of sturdy cardboard over the front panel for protection.

4. Place the counter into a plastic bag and seal the bag.

5. Wrap the bagged instrument and accessories in one inch thick flexible cellular plastic film cushioning material (per PPP-C-795) and place in a barrier bag (per MIL-B-131). Extract the air from bag and heat seal.

6. Place bagged instrument and accessories into an oversized card-board box (per PPP-B-636 type CF, class WR, variety SW, grade V3C). Fill additional spaces with rubberized hair or cellular plastic cushioning material. Close box in accordance with container specifications. Seal with sturdy water resistant tape or metal straps.

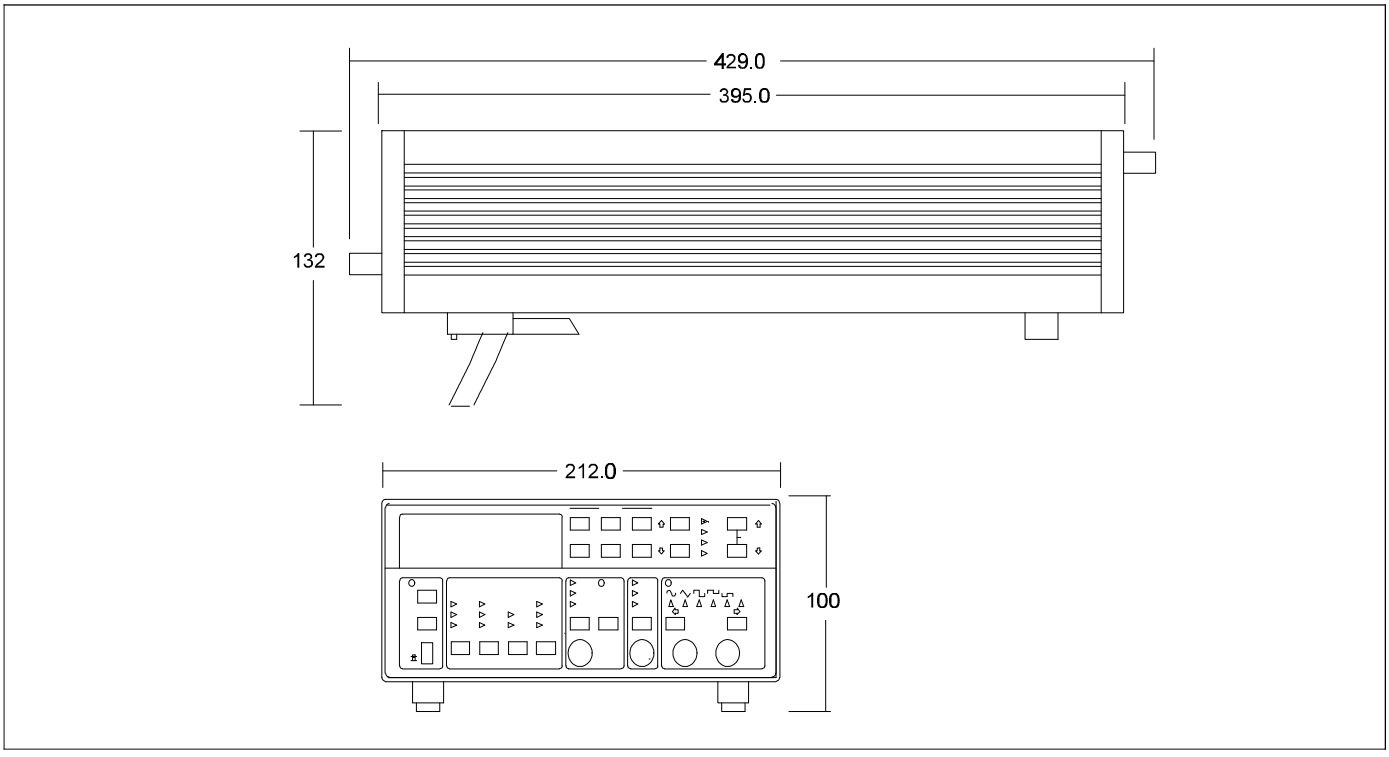

Figure 2-2. Model 8550/8551 - Outline Dimensions.

7. Mark container “DELICATE INSTRUMENT”, “FRAGILE”, etc. Mark instrument model and serial number and date of packaging. Affix shipping labels as required or mark according to MIL-STD-129.

NOTE

If the instrument is to be shipped to Tabor for calibration or repair, attach a tag to the instrument identifying the owner. Note the problem, the symptoms, and service or repair desired. Record the model and serial number of the instrument. Show the work authorization order as well as the date and method of shipment. ALWAYS OBTAIN A RETURN AUTHORIZATION NUMBER FROM THE FACTORY BEFORE SHIPPING THE INSTRUMENT TO Tabor.

2-12. SAFETY

Be fully acquainted and knowledgeable with all aspects of this instruction manual before using the instrument to assure operator safety and protection against personnel shock hazard.

Operating Instructions Section 3

3-1. INTRODUCTION

Model 8550/8551 operation is divided into two general categories: basic bench operation, and IEEE-488 operation. Basic bench operation, which is covered in this section, explains how to use the model 8550 for generating the required waveform characteristics. IEEE programming can also be used to greatly enhance the capability of the instrument in applications such as automatic test equipment. This aspect is covered in details in Section 4.

3-2. FRONT PANEL FAMILIARIZATION

The front panel is generally divided into three sections: controls, connectors, display and indicators. The following paragraphs describe the purpose of each of these items in details.

3-2-1. Controls

All front panel controls except POWER are momentary contact switches. Most controls include an annunciator light for indication of the selected parameter and operating mode. Some controls do not have an annunciator light. Exercising these controls generates an immediate response on the display.

Front panel controls may be divided into functional groups: Operating mode, State, Main Parameters, Trigger Mode, Control, Output and Modifiers.

3-2-1-1. Operating Mode

Two push-buttons in the operating mode group provide selection between four operating modes. Selection of one of the operating modes is done by depressing one of these buttons. The selected mode is indicated by an LED.

3-2-1-2. State

Three push-buttons are included in the status group. The function of each of these buttons is described in the following.

POWER - The POWER switch controls the AC power to the instrument. Pressing and releasing the switch once turns the power on. Pressing and releasing the switch a second time turns the power off.

2nd/EXE - Several push-buttons were assigned a second function which are only accessible after the [2nd] button was depressed. These functions are marked below the buttons in blue script. Some second functions require that the [EXE] push-button be pressed again before the function is executed.

LCL/P.SET/DCL - The LCL/P.SET push-button when depressed, and the instrument is in its remote mode (but not in remote lockout condition LLO), restores the instrument to its local operating mode. When the generator is in its local operating mode, depressing this push-button restores only the currently displayed parameter to its factory pre-set value, other parameters are not affected by pressing this button. Front panel P.SET values are listed in Table 3-1. A third function is also assigned to this switch. Depressing this push-button after the [2nd] button consequently modifies front panel set-up to its factory default. The function of DCL is described in details in paragraph 3.5.

3-2-1-3. Main Parameters - Model 8550

There are four MAIN PARAMETERS push-buttons which are used to modify the displayed reading. Each time a button is depressed a different parameter is displayed. The selected parameter is indicated by an LED. Each row of LEDs is associated with a specific operating mode. The parameters in the following may be displayed and modified. Table 3-2 lists the limits for each of the above parameters.

1. FUNCTION

FREQ - Frequency of the selected output waveform. Frequency is defined for repetitive signals only. When the function generator is set to operate in

triggered mode, the programmed frequency value has no effect on the output. In gated mode, the frequency defines the repetition rate within the gating signal. In sweep mode, the programmed value defines the sweep start point. The programmed frequency retains its value at both SYNC and the main output connectors. The frequency parameter may be programmed within the range of 10.00mHz to 50.00MHz. Preset value is set to 1.000KHz.

AMPL - Amplitude of the selected waveform at the main output connector. The output signal is driven from a 50Ω source therefore, the value of the amplitude parameter is specified and accurately controlled only when the output is terminated with 50Ω. If the signal from the output connector is connected to an high impedance circuit, the actual amplitude level at the output connector is doubled. Amplitude control has no effect on the amplitude level at the SYNC output connector. The amplitude parameter may be programmed within the range of 10.0mV to 16.0V. Preset value is set to 1.00V.

OFST - DC offset of the selected waveform at the main output connector. Similarly to the amplitude, the offset parameter is specified and accurately controlled only when the output is terminated with 50Ω. Offset control has no effect on the SYNC output connector. The offset parameter may be programmed within the range of 0.00mV to ±7.95V. Preset value is set to 0mV.

2. SWEEP

STOP - Defines the sweep stop frequency. When the function generator is set to operate with one of its sweep modes, the waveform at the output connector sweeps from frequency set by the FREQ setting to that set by the STOP frequency. In several sweep modes sweep stop may change its function to sweep start. The programmed frequency retains its value at both SYNC and the main output connectors. If the instrument is set to operate in logarithmic sweep mode, the sweep stop parameter may be programmed within the range of 10.00mHz to 50.00MHz. In linear sweep mode the sweep stop parameter may only programmed within three decades from the start frequency setting. Preset value is set to 9.000KHz.

TIME - In linear sweep mode, sweep time determines the time that it takes for completing one sweep cycle. Sweep time is different for logarithmic sweep mode where the specified value is that required for sweeping one decade. The generator may be set to sweep over 10 decades. In that case, the sweep time should be multiplied by ten. Decade size ranges from 1000 to 9999 counts (or 100:1 if settings other than full and minimum scales are required). If only part of the decade is being swept, the sweep time is reduced proportionally. The sweep time parameter may be programmed within the range of 10ms to 999s. Preset value is set to 1.00s.

MARK - Specifies the frequency of which the sweep marker changes its voltage level at the marker output connector. The marker output is only active when the function generator is set to operate with one of its built-in sweep modes. The sweep marker parameter may be programmed within the same range as the frequency stop parameter. Preset value is set in both linear and logarithmic modes to 5.000KHz.

3. PHASE OFFSET

PLL - The Model 8550 output may be locked to an external signal. The operator may then introduce a phase offset between the leading edge of the external signal and the leading edge of the signal at the output connector. The phase offset is programmed with the PLL parameter. The phase offset parameter may be programmed within the range of ±180°. Preset value is set to 0°.

TRIG - The TRIG parameter inserts a phase offset between the triggering signal and the generated output signal. The trigger phase offset has no effect on external signals having a high slew rate, such as square waves. The trigger phase offset parameter may be programmed within the range of ±90°. Preset value is set to 0°.

4. TRIGGER

PER - A built-in generator provides an internal triggering stimulant in such cases where an external signal is not available. The displayed value specifies the interval between consecutive triggering sequences. The trigger period parameter may be programmed within the range of 20µs to 999s. Preset value is set to 1.00s.

BUR - Model 8550 has the capability of generating a burst of waveforms, at its output connector, having an exact number of complete cycles. The counted burst function operates on all output waveforms except on DC output. The burst of counted number of output cycles can be programmed within the range of 1 to 4000 output cycles. Preset value is set to 2 cycle.

LEVEL - The LEVEL parameter sets the trigger voltage level at the TRIG INPUT connector. The output signal will trigger the function generator at the point set by LEVEL parameter. The trigger level parameter may be programmed within the range of −10.0V to +10.0V. Preset value is set to 1.6V.

3-2-1-3A. Main Parameters - Model 8551

There are four MAIN PARAMETERS push-buttons which are used to modify the displayed reading. Each time a button is depressed a different parameter is displayed. The selected parameter is indicated by an LED. Each row of LEDs is associated with a specific operating mode. The parameters in the following may be displayed and modified. Table 3-2 lists the limits for each of the above parameters.

1. FUNCTION

FREQ - Frequency of the selected output waveform. Frequency is defined for repetitive signals only. When the function generator is set to operate in triggered mode, the programmed frequency value has no effect on the output. In gated mode, the frequency defines the repetition rate within the gating signal. In sweep mode, the programmed value defines the sweep start point. The programmed frequency retains its value at both SYNC and the main output connectors. The frequency parameter may be programmed within the range of 10.00mHz to 50.00MHz. Preset value is set to 1.000KHz.

AMPL - Amplitude of the selected waveform at the main output connector. The output signal is driven from a 50Ω source therefore, the value of the amplitude parameter is specified and accurately controlled only when the output is terminated with 50Ω. If the signal from the output connector is connected to an high impedance circuit, the actual amplitude level at the output connector is doubled. Amplitude control has no effect on the amplitude level at the SYNC output connector. The amplitude parameter may be programmed within the range of 10.0mV to 16.0V. Preset value is set to 1.00V.

OFST - DC offset of the selected waveform at the main output connector. Similarly to the amplitude, the offset parameter is specified and accurately controlled only when the output is terminated with 50Ω. Offset control has no effect on the SYNC output connector. The offset parameter may be programmed within the range of 0.00mV to ±7.95V. Preset value is set to 0mV.

P.OFST - The Model 8551 output may be locked to an external signal. The operator may then introduce a phase offset between the leading edge of the external signal and the leading edge of the signal at the output connector. The phase offset is programmed with the P.OFST parameter. The phase offset parameter may be programmed within the range of ±180°. Preset value is set to 0°.

2. PULSE

PER - Similar to the FREQ parameter, the PER sets the period of the selected output waveform. Period is defined for repetitive signals only. When the pulse/function generator is set to operate in triggered mode, the programmed period value has no effect on the output. In gated mode, the period defines the repetition rate within the gating signal. The programmed period retains its value at both SYNC and the main output connectors. The period parameter may be programmed within the range of 20.00ns to 99.99s. Preset value is set to 1.000ms.

WIDTH - The pulse width parameter defines the time interval between two consecutive transitions; positive to negative transition in normal output mode or negative to positive transition in pulse complement mode. The width parameter is common to the pulse and the ramp waveforms. It is convenient to interpret the displayed and specified value as that obtained with the fastest edges. However, In linear transition mode, the displayed and specified value is that obtained at the turning point of the pulse edges. The pulse width parameter may be programmed within the range of 10.0ns to 999ms. The ramp width parameter may be programmed within the range of 5.00µs to 999ms. Preset value is set for both the pulse width and the ramp width to 100µs.

DUTY - The DUTY parameter specifies the duty cycle of either the pulse output or the ramp output, when the Model 8551 is set to operate in its fixed duty cycle mode. The duty cycle parameter may be programmed within the range of 1% to 8550%. Preset value is set 50%.

3. TRANSITION

LEAD - The LEAD parameter specifies the time interval between the 10% to 90% amplitude points on the leading edge. The leading edge value may only be selected when the pulse/function generator is set to operate in its linear transition mode; otherwise, the leading edge transition time is set to its fastest position. The leading edge transition time

parameter may be programmed within the range of 8ns to 99.9ms. Preset value is set 10.0µs.

TRAIL - The TRAIL parameter specifies the time interval between the 10% to 90% amplitude points on the trailing edge. The trailing edge value may only be selected when the pulse/function generator is set to operate in its linear transition mode; otherwise, the trailing edge transition time is set to its fastest position. The trailing edge transition time parameter may be programmed within the range of 8ns to 99.9ms. Preset value is set 10.0µs.

4. TRIGGER

PER - A built-in generator provides an internal triggering stimulant in such cases where an external signal is not available. The displayed value specifies the interval between consecutive triggering sequences. The trigger period parameter may be programmed within the range of 20µs to 999s. Preset value is set to 1.00s.

BUR - Model 8551 has the capability of generating a burst of waveforms, at its output connector, having an exact number of complete cycles. The counted burst function operates on all output waveforms except on DC output. The burst of counted number of output cycles can be programmed within the range of 1 to 4000 output cycles. Preset value is set to 2 cycles.

LEVEL - The LEVEL parameter sets the trigger voltage level at the TRIG INPUT connector. The output signal will trigger the function generator at the point set by LEVEL parameter. The trigger level parameter may be programmed within the range of –10.0V to +10.0V. Preset value is set to 1.6V.

PHASE - The PHASE parameter inserts a phase offset between the triggering signal and the generated output signal. The trigger phase offset has no effect on external signals having a high slew rate, such as square waves. The trigger phase offset parameter may be programmed within the range of ±90°. Preset value is set to 0°.

3-2-1-4. Trigger Mode

Two push-buttons are grouped in the TRIGGER MODE section. Selection of one of the trigger modes is done by depressing one of these buttons. The selected mode is indicated by an LED. Model 8550 may be triggered from either one of the following sources:

1. External signal which may be applied to the TRIG/REF IN connector
2. An internal - asynchronous trigger generator
3. GPIB commands (like GET or *TRG)
4. Front panel [MANual] push-button

The [MANual] trigger is active when the instrument set to operate in one of its external trigger modes. This push-button when depressed serves as a replacement for an external trigger source.

3-2-1-5. Control

There is one push-button in the MOD group. This button is used to select an external modulation control for the function generator. The selected control mode is indicated by an LED.

3-4-1-6. Output

There are two push-buttons in the OUTPUT group. These buttons are used for selecting an output waveforms for the output connector. The selected function is indicated by an LED.

Note

The Model 8550 powers up with its output in stand by state. You have to press one of the two push-buttons in the OUTPUT group to remove the Model 8550 from stand by.

3-4-1-7. Modifier

The MODIFIER push-buttons simulate digital potentiometers. The MODIFIER push-buttons operate in conjunction with the MAIN PARAMETER group. There are four sets of modifying buttons. Three sets are dedicated for changing the displayed read-out. The two push-buttons which are marked RANGE are used to change the range of the displayed parameter.

3-2-2 Connectors

The connectors are used for connecting the Model 8550 to the unit under test, to a control device, and to an external triggering stimulant.

1. TRIG/REF INPUT - The TRIG/REF INPUT connector is used for applying an external triggering source to the function generator. The same connector is used in conjunction with the phase lock operating mode; the reference signal is applied to this connector.

2. MOD INPUT - The MOD INPUT connector is used for applying external controlling signals to the

Table 3-1. Default States After Software Reset

FUNCTION	DESCRIPTION	DEFAULT STATE
Function Parameters		
FREQ	Frequency	1.000KHz
AMPL	Amplitude	1.00V
OFST	Offset	0mV
Sweep Parameters		
STOP	Sweep Stop Frequency	9.000KHz
TIME	Sweep Time	1.00s
MARK	Sweep Marker Frequency	5.000KHz
Phase Parameters		
PLL (Model 8550)	Phase Lock Offset	0°
P.OFST (Model 8551)	Phase Lock Offset	0°
TRIG (Model 8550)	Start Trigger Phase Offset	0°
Trigger Parameters		
PER	Internal Trigger Period	1.00s
BUR	Counted Burst	2 cycles
LEVEL	Trigger Level	1.6V
PHAS (Model 8551)	Start Trigger Phase Offset	0°
Pulse/Ramp Parameters		
PER (Model 8551)	Period	1.000ms
WIDTH (Model 8551)	Pulse/Ramp Width	10.0s
DUTY (Model 8551)	Duty Cycle	50%
Operating Mode	Main Operating Mode Selection	Normal Function Generator
State	GPIB Status	Local state
Display	Displayed Parameter	Frequency
Trigger Mode	VCO stimulant	Internal, Continuous Mode
Control	Carrier Modulation Control	Off
Output	Output Waveform	Sinewave
ST. BY	Output Stand By	On (no output)

function generator. Model 8550 accepts VCO, amplitude and frequency modulating signals, while Model 8551 accepts additional pulse width modulating signal.

3. SYNC OUT - The SYNC OUT connector outputs fixed amplitude pulses from a 50Ω source. The leading edge of the SYNC output is synchronous with the leading edge at the main output connector.

4. OUT - The OUT connector is used as the main output for the function generator. Output is driven from a 50Ω source. Special care should be taken when these outputs are connected to the device under test because these outputs are capable of delivering up to 32Vp-p. For safety reasons, after power on or after software reset, the OUT connector is disconnected from the output circuit. To resume normal operation press one of the two buttons above the OUT connector.

3-2-3. Display And Indicators

1. DISPLAY - The function of the numeric display is to indicate the value of the various parameters. The display consists of a 4 digit mantissa and a single digit exponent. The exponent uses a leading minus indicating negative values. The sign on the exponent changes to + for zero or positive values.

The display is also used to indicate other information such as messages.

2. INDICATORS - 35 indicators are located on the front panel (Model 8551). These indicators are used as pointers to a selected parameter, operating modes, trigger modes etc.

3-3. REAR PANEL FAMILIARIZATION

3-3-1. Connectors And Switches

1. AC RECEPTACLE - Power is applied through the supplied power cord to the 3-terminal AC receptacle. Note that the selected ac mains voltage is marked on the line voltage selector switch.

2. LINE SWITCH - The LINE VOLTAGE SELECTOR switch selects one of the primary voltage which are marked on both sides of the switch.

3. LINE FUSE - The line fuse provides protection for the AC power line input. For information on replacing this fuse, refer to Section 5.

4. IEEE-488 CONNECTOR - This connector is used for connecting the instrument to the IEEE-488 bus.

5. SWEEP OUT CONNECTOR - This connector is used for connecting the instrument the X input on the oscilloscope. Its output level is either fixed - in linear sweep mode, or proportional to the sweep time per decade - in logarithmic sweep mode.

6. MARKER OUTPUT CONNECTOR - This connector is used for connecting the function generator to the Z input on the oscilloscope. This output is only active when sweep mode is on.

3-4. POWER-UP PROCEDURE

The basic procedure of powering up the Model 8550 is described below.

1. Connect the female end of the power cord to the AC mains receptacle on the rear panel. Connect the other end of the power cord to a grounded AC outlet.

WARNING

Be sure the power line voltage agrees with the indicated value on the rear panel of the instrument. Failure to heed this warning may result in instrument damage.

The instrument is equipped with a 3-wire power cord designed to be used with grounded outlets. When the proper connections are made, the instrument chassis is connected to the power line ground. **Failure to use a properly grounded outlet may result in personal shock hazard.**

2. Turn on the mains power by pressing and releasing the POWER switch on the front panel.

3. The instrument then begins operation by performing a display and indicator test which takes approximately one second. All front panel indicators turn on and the display appears as follows:

8.8.8.8.(8

4. To verify that all display segments are operating, compare the instrument's display with the above during the test.

5. After all the indicators are tested, the instrument performs ROM and RAM tests. Successful execution of these tests is followed by a one second read-out of the installed software revision, similar to the example below:

So1.0

6. Following the software revision level, the instrument proceeds with displaying the previously selected GPIB primary address. The GPIB address is set by front panel programming and is stored in the non-volatile memory. For example, with the generator programmed to address 18, the display shows:

GP18

7. Following these display messages, the instrument commences its normal operating mode and generates waveforms. Note that the instrument is equipped with a non-volatile memory. This memory automatically monitors front panel traffic and retains its latest set-up for events such as accidental power loss. In case of power loss the instrument resumes operation with its previously programmed front panel set-up.

NOTE

One who does not wish to observe the power-up procedure every time that the generator is turned on, can easily remove the sequence of displayed messages. Depressing [2nd] and then [Operating Mode ⇑] in sequence writes a special code to the non-volatile memory. The next time

the generator will be powered-up, the instrument will skip the power-up procedure and will immediately commence with displaying the front panel set-up. repeating the sequence of [2nd] and [Operating Mode ⇑] restores normal power up procedure. Note that there are no front panel markings that indicate power-up sequence removal. Therefore, unless the instrument is being used by one person only, and to remove confusion, it is recommended that power-up sequence remains unchanged.

3-5. SOFTWARE RESET

An operator who is not yet fully familiar with front panel operation of the function generator, may find himself locked into a "dead-end" situation where nothing operates the way it should. The fastest way of restoring the generator to a known state is by resetting its software. This may be done by pressing the [2nd] push-button and then pressing the [DCL] push-button (second function to the [LCL/P.SET] push-button). The instrument then resets to its factory selected defaults. Table 3-1 summarizes these defaults.

3-5-1. Parameter Preset

As discussed in paragraph 3-5, software reset restores all front panel parameters to their factory selected values. It may, however, be required to preset one or two parameters and leave the rest intact. In that case the instrument provides additional capabilities with its [P.SET] (preset) function. Depressing [LCL/P.SET] push-button modifies the displayed parameter to its default value. Default values are summarized in Table 3-1.

NOTE

Software reset has no effect on the stored front panel set-ups. Software reset also has no effect on the programmed GPIB address.

3-6. DISPLAY MESSAGES

Model 8550 has several display messages pertaining to its operation. The generator also displays an error indication when a front panel programming error is detected. These messages and error indications are discussed in the following. Note that the instrument has a number of additional display messages associated with IEEE-488.2 programming. These messages are discussed in section 4 of this manual.

3-7. DETECTING PROGRAMMING ERRORS

Model 8550 is a product of many years of experience and complete understanding of human engineering requirements. A great deal of time was devoted during its design stage to simplify front panel programming procedures, thereby minimizing the potential of programming errors. It is impossible however for an inexperienced operator to completely avoid programming errors. For such cases, the function generator employs a built-in error detection mechanism which warns against programming errors.

There are several error indications that may occur due to incorrect front panel programming procedures. The indications are either visible (error messages) or audible (beeping sound). The audible alarm sounds while attempting an incorrect front-panel programming sequence. For instance, an attempt to program an offset which exceeds the level window limits is a cause for such an alarm. The alarm sound as long as the conditions remain false. Other error conditions which may cause an audible alarm are discussed in different parts of this manual.

Front panel programming errors are normally indicated by an audible alarm. GPIB errors are detected automatically and are screened for a service request poll. These indications are described in the following paragraphs.

3-8. FRONT PANEL ERROR INDICATION

In general, whenever a front panel or GPIB programming attempts to place the 8550 in an error condition, the Model 8550 responds by front panel error indication or by addressing the IEEE-488.2 service request register.

Errors are categorized in four main groups:

1. General errors
2. Limit errors
3. Pulse/Ramp setup errors
4. IEEE errors
5. Auto-Calibration errors

3-8-1. General Errors

Errors in this group are caused by improper usage of the instrument. Such errors occur while attempting to place the instrument in an illegal mode. For example, depressing simultaneously two push-buttons

(except [AUTOCAL]) has no valid definition or by depressing the MANUAL push-button while the instrument is in its continuous operating mode. In such cases, the instrument sounds an audible alarm, ignores this error, and continues with its normal operation.

3-8-2. Limit Errors

Errors in this group are caused by an attempt to program values outside the legal limits of the instrument. The instrument automatically rejects any attempt to program such parameters, sounds an audible alarm, and then resumes normal operation. Table 3-2 summarizes all front panel entry limits.

3-8-3. Pulse/Ramp Set-up Errors (Model 8551 only)

The pulse/ramp setup errors are inter-parameter inconsistencies errors, such as pulse width greater than the selected period. The pulse generator tests the programmed parameter every time that a modifier push-button is depressed. Programming the Model 8550 with pulse/ramp errors is possible and executable however, when such errors are detected, the ERROR light starts blinking; indicating that the signal at the output connector may emerge with other parameters then those programmed. The light error blinks until the error conditions are removed. Pulse/ramp error summary is given in Paragraph 4-14-4.

Pulse/Ramp errors may occur under one or more of the following conditions:

1. The programmed pulse/ramp WIDTH parameter is greater than the selected period.

2. Model 8551 is placed in linear transition time and one of the programmed transitions is greater than the selected pulse width.

3. Model 8551 is placed in internal triggered mode and the programmed pulse/ramp width is greater than the selected internal trigger period.

4. The programmed ramp width is outside the limit of 5.00µs.

5. The programmed pulse width is outside the specified limits.

3-8-4. IEEE-488.2 Errors

In general, whenever a GPIB programming attempts to put the model 8550 into an error condition, the function generator responds in two ways. First by displaying a front panel message and than, if programmed so, by raising an SRQ flag in its Status Byte Register. Using the serial poll command, the controller may then address the generator and request its status byte.

The generator incorporates a number of display messages which are associated with errors involving GPIB interface programming. These messages are discussed in detail in Section 4 of this manual.

There is one message however, which should be explained at this point because it may interfere with front panel operation. A remote enable or a device dependent command sent to the instrument through the bus turns the REMOTE light on. In this case, all front panel push-buttons except [LCL] are disabled. Press one of these push-buttons causes the function generator to respond with the following message:

LcL

This message indicates that the instrument expects that the [LCL] push-button be first depressed otherwise front panel operation is ignored. After the [LCL] button is depressed, the REMOTE light turns off and the instrument is ready to accept further front panel programming sequences.

3-8-5. Auto-Calibration Errors

Model 8550 provides an auto-calibration function which may be used by the operator. In the event that the calibration routine fails to successfully complete, the generator generates a calibration failure list and starts displaying the following message:

FAIL d

Where d represents blinking digits in the range of 1 to 9. A function LED indicator - in the MAIN PARAMETERS, blinks simultaneously; indicating the area where the generator failed to calibrate. Operating the auto-calibration function and interpreting the generated failure list are described later in this manual. The auto-calibration failure list is also available as a GPIB failure status query.

3-9. SELECTING 2nd FUNCTIONS

A few front panel push-buttons were assigned a secondary function. These functions are marked below the button in blue color and are accessible through the [2nd] push-button.

There are ten front panel buttons which were assigned a secondary function. These functions are:

DCL **STORE**

RECALL	**SWP MODE** (Model 8550)
GPIB ADR	**LIN/FIXED** (Model 8551)
RCL MODE	**INT TRG**
STANDBY	**COMPL** (Model 8551)
FAIL LIST	

The operation of these secondary functions is described later in this chapter. Pressing the [2nd] push-button generates the following display read-out:

2nd ?

The question mark (?) appears blinking; indicating that the instrument is ready for a consequent press of another push-button which was assigned a secondary function. Depressing [2nd] once more cancels this function. Second functions: DCL, SWP MODE, LIN/FIXED/ INT TRG, ST-BY, and COMPL function are executed immediately; STORE, RECALL, GPIB ADR, RCL MODE, and FAIL LIST will be executed only after depressing the [EXE] push-button.

3-10. AUTO-CALIBRATION

Model 8550 provides an auto-calibration function that may be operated at any time, either from the front panel or through a GPIB command. Operating the auto-calibration is very simple and can be done by anyone; no special skills are required. Although this function can give the user relative confidence that the instrument is operational and within specification, it is still recommended that the function generator will be checked periodically by certified calibration laboratories. Suggested calibration period by certified calibration laboratories is given in Section 5 of this manual. The auto-calibration takes only few seconds to complete. It therefore could be used often without serious delay to its normal operation. However, the auto-calibration function **must be** operated when one or more of the following conditions occur:

1. After 30 minutes of warm-up time;
2. After 24 hours of last internal auto-calibration;
3. If ambient temperature changes by more than 5°C, and;
4. After replacing components or sub-assemblies.

To operate the auto-calibration function proceed with the following steps:

PARAMETER	LOW LIMIT	HIGH LIMIT	REMARKS
FRQ (frequency)	10.00mHz	50.00MHz	
AMP (amplitude)	10.0mV	16.0V	Into 50Ω
OFS (offset)	0.0mV	±795mV	Within a ±800mV level window
OFS (offset)	0mV	±7.95V	Within a ±8.00V level window
PLL (phase offset)	0°	±180°	
PER (period)	99.99s	20.00ns	Model 8551 only
WID (pulse/ramp width)	999ms	10.0ns	Model 8551 only
DTY ((duty Cycle)	1%	8550%	Model 8551 only
LEE (leading edge)	99.9ms	8ns	Model 8551 only
TRE (trailing edge)	99.9ms	8ns	Model 8551 only
RPT (internal trigger period)	999s	20µs	
BUR (counted burst)	1	4000	
TLV (trigger level)	0.0mV	±10.0V	
TPH (trigger phase offset)	0°	±90°	
DCO (dc output level)	0.0mV	8.00V	Model 8550 only
STP (log sweep stop)	10.00mHz	50.00MHz	Model 8550 only
SSN (lin sweep stop)	10 display counts	5000 display counts	Model 8550 only
SWT (sweep time)	10ms	999s	Model 8550 only
MRK (log marker freq)	10.00mHz	50.00MHz	Model 8550 only
MKN (lin marker freq)	10 display counts	5000 display counts	Model 8550 only
*SAV (store)	00	30	
*RCL (recall)	00	30	

Tabel 3-2. Front Panel Parameter Entry Limits

1. Depress the POWER switch once to turn power on, and leave the instrument on at least 30 minutes until the internal circuits reach thermal equilibrium.

2. Depress the two [AUTOCAL] push-buttons simultaneously, and observe that the generator displays the following:

CAL ?

The "?" appears blinking; indicating that the instrument has not yet commenced with its calibration routine. Depress any front panel push-button to quit the auto-calibration sequence and return to normal operation. Depressing [EXE] initiates the calibration routine. The blinking question mark is then replaced by a moving bar. The bar circles as long as the calibration routine is in process.

Following successful execution of its internal calibration, the instrument resumes normal operation. If self calibration fails, the generator proceeds with displaying a failure list. Recalling and terminating the failure list display is described in the succeeding paragraph. Analyzing and interpreting the failure list is described in Section 5.

3-11. REVIEWING THE AUTO-CALIBRATION FAILURE LIST

As discussed above, if the auto-calibration fails to successfully complete, the instrument automatically generates a failure list. The operator can review this list either immediately after the auto-calibration process or anytime later provided, however, that a subsequent calibration process did not remove one the previously generated errors.

If the auto-calibration completes without detecting a calibration error, no failure list is generated and the function generator resumes normal operation. If a calibration error is detected, the generator starts displaying a message as described in paragraph 3-8-5.

To terminate this display message and to exit from the failure evaluation process depress any front panel push-button. To evaluate the complete failure list depress the [FAIL LIST ⇑] or the [FAIL LIST ⇓] push-buttons. The blinking LED and the associated displayed digit indicates where the instrument has some difficulties to calibrate itself.

To recall the last saved failure list depress the [2nd] and the [FAIL LIST ⇓] push-buttons in sequence and observe that the instrument displays the message as described in paragraph 3-8-5. Commence with the evaluation using the same procedure as was described above.

3-12. MODIFYING PARAMETERS

There are various parameters, such as frequency and amplitude, which control the shape of the waveform at the output connector. Modification of a specific parameter is simply done by pressing the push-button below the requested parameter until the light behind the required parameter illuminates. At this time the numeric readout displayed a value plus an exponent. For example, a FREQ readout of 10.00 (exp)+3 tells us that the output waveform is programmed to have a frequency of 10.00 KHz. Limits for each parameter are given in Table 3-2. The parameter can be modified using the [MODIFIER] and the [RANGE] push-buttons.

The parameters which can be modified are marked on the front panel as follows:

Function parameters:

FREQ	(Frequency)
AMPL	(Amplitude)
OFST	(Offset)
PHASE	(PLL offset - Model 8551)

Sweep parameters (Model 8550 only):

STOP	(Sweep stop frequency)
TIME	(Sweep time)
MARK	(Marker frequency)

Pulse parameters (Model 8551 only):

PER	(Period)
WIDTH	(Pulse width)
DUTY	(Duty cycle)

Phase offset Parameters:

PLL	(PLL offset - Model 8550)
TRIG	(Trigger phase offset)

Transition times parameters (Model 8551 only):

LEAD	Leading edge
TRAIL	Trailing edge

Trigger parameters:

PER	(Int. trigger period)
BUR	(Burst count)
LEVEL	(Trigger level)
PHASE	(Trig phase - Model 8550)

In addition, some parameters are accessible through the [2nd] button. These parameters are:

STORE	(Store address)
RECALL	(Recall address)
SWP MODE	(Sweep mode/direction)
GPIB ADR	(GPIB address)

3-12-1. Using the Modifier

The modifier group consists of three sets of push-buttons - each having its top button marked with an arrow pointing up (⇑) and its bottom key marked with an arrow pointing down (⇓). These modifier push-button control the displayed readout within a selected range.

The [x1 ⇑] or [x1 ⇓] push-buttons when depressed and released once increment or decrement the least significant digit on the numeric display. Depressing these buttons for more than one second modifies this digit constantly until the button is released or until the parameter limit is encountered. Incrementing the [x1] above 9 carries 1 to the second digit.

The [x10 ⇑] or [x10 ⇓] push-buttons control the second digit. Their operation is similar to the [x1] operation. Incriminating the [x10] above 9 carries 1 to the second digit.

The [x100 ⇑] or [x100 ⇓] push-buttons control the third and the fourth (most significant) digit.

3-12-2. Modifying the Range

The [RANGE] buttons control the range of the displayed parameter. Depressing and releasing the [RANGE ⇑] or the [RANGE ⇓] buttons increases or decreases respectively the displayed range. Depressing these buttons when the generator is already at its highest or lowest range produces no further change.

3-12-3. Parameter Limits

In general, parameters were assigned definite boundaries. The instrument was design in such a way that front panel programming, under no circumstances, may lead to an error situation by exceeding the specified limits. GPIB parameter programming errors are discussed in section 4. Front panel programming permits modification of parameters within the limits which are given in Table 3-2. Note that the modifier buttons [x1], [x10] and [x100] can only modify a parameter within one range. These buttons in conjunction with the [RANGE] push-button may cover the entire specified range.

3-13. SELECTING AN OPERATING MODE - MODEL 8550

Model 8550 may operate as a function generator, as a sweep generator (linear or logarithmic), and as a phase locking generator. Selecting one of the operating modes is done by depressing one of the OPERATING MODE [⇑ or ⇓] push-buttons until the light behind the desired mode illuminates.

Description of the various modes which can be used Model 8550 is given in the following.

3-13-1. Normal Function Generator Operating Mode - Model 8550

Function generator operating mode is the normal operating conditions where the output waveform is symmetrical about its horizontal and vertical axis. The normal operating mode also permits a vertical offset of its output waveform. The generator is placed in its normal operating mode when the light behind FUNC illuminates. Triggered operation and externally controlled modes such as VCO, FM, and AM may operate in conjunction with the normal function generator operating mode.

3-13-2. Linear/Logarithmic Sweep Operating Mode - Model 8550

Placing the model 8550 in linear or logarithmic sweep operating mode transforms the instrument into an independent sweep generator. The function generator has eight built-in sweep modes of which four of them are linear sweep modes and four are logarithmic. Select between linear or logarithmic sweep mode by depressing the OPERATING MODE [⇑ or ⇓] push-buttons until the light behind the desired mode illuminates. The various sweep modes may operate in conjunction with the triggered modes.

3-13-2-1. Selecting Sweep Direction

When Model 8550 is placed in sweep mode (linear or logarithmic), the selected waveform at the output connector repeatedly changes its frequency in a direction set by the sweep start (FREQ) parameter to frequency set by the sweep stop (STOP) parameter. The time for completing one sweep cycle is determined by the sweep time (TIME) parameter. There are four different directions that the output waveform may sweep to. The difference between the various

modes is more significant when using the triggered sweep mode as described in the following:

SWEEP UP - The function generator, when triggered, sweeps from value set by FREQ to value set by STOP. Sweep time is determined by TIME. At the end of the sweep, the output waveform remains at the stop frequency. Following another trigger, the output jumps quickly to its start frequency and the above cycle is repeated. In normal mode the generator repeats its sweep cycle continuously.

SWEEP DN - The sweep down mode is similar to the sweep up mode except that the output waveform, when triggered, sweeps from frequency set by the sweep stop (STOP) parameter to frequency set by the sweep start (FREQ) parameter. Sweep time is determined by the TIME parameter. At the end of the sweep, the output waveform remains at the start frequency. Following another trigger, the output jumps quickly to its stop frequency and the above cycle is repeated. In normal mode the generator repeats its sweep cycle continuously.

SWEEP UP-DN - The function generator, when triggered, sweeps from value set by the FREQ parameter to value set by the STOP parameter and back to the FREQ value. Sweep time is doubled than the displayed TIME parameter. At the end of the sweep, the output waveform remains at the start frequency. Following another trigger, the above cycle is repeated. In normal mode the generator repeats its sweep cycle continuously.

SWEEP DN-UP - The sweep down mode is similar to the sweep up mode except that the output waveform, when triggered, sweeps from value set by the STOP parameter to value set by the FREQ parameter and back to the STOP value. Sweep time is doubled than the displayed TIME parameter. At the end of the sweep, the output waveform remains at the stop frequency. Following another trigger, the above cycle is repeated. In normal mode the generator repeats its sweep cycle continuously.

Selecting one of the above sweep directions is described in the following. The same procedure is used for both linear and logarithmic sweep scales.

1. Depress the [2nd] push-button and observe that the display is modified to indicate the following:

2nd ?

(? appears flashing)

2. Depress the [SWP MODE] push-button in the MAIN group and observe that one of the following read-outs is displayed:

UP, dn, U-d or d-U

This reading indicates the selected sweep mode. To modify the selected sweep mode to your desired modes depress the [x1 ⇑] modifier push-button until the selected mode is displayed.

3. Depress the [EXE] push-button. The output waveform now sweeps with the selected sweep mode.

3-13-3. Phase Locking Generator Operating Mode - Model 8550

Model 8550 employs an automatic locking circuit which enables phase and frequency locking to an external reference. Model 8550 locks on the external reference signal regardless of its programmed frequency setting. After the generator has locked on the signal, the user may generate a phase offset between the external signal and the signal at the output connector. Offset range is ±180°. The generator is placed in its phase locking operating mode when the light behind PLL illuminates. The phase locking operating mode can not be operated in conjunction with the triggered modes. To operate the instrument in its PLL operating mode proceed as follows:

1. Depress the [POWER] switch once to turn the power on.

2. Depress the operating mode push-buttons until the light behind PLL illuminates.

3. Modify trigger level parameter (TRIG LEVEL) to the required thrash-hold level.

4. Connect a BNC cable from the reference source to the front panel REF INPUT connector. Use a “T” connector and connect the reference signal to channel A on an oscilloscope.

5. Connect a BNC cable from 8550 output to channel B on the oscilloscope.

6. Set oscilloscope and observe that the two signals have the same frequency and are locked on the same phase.

3-13-3-1. Generating Phase Offsets

As discussed in paragraph 3-12-3, the generator is capable of generating phase offsets between the external reference signal and the main output connector. To generate phase offset proceed as follows:

1. Repeat the operating instruction as in the previous paragraph.
2. Depress the [PHASE OFFSET] push-button until the light behind PLL illuminates.
3. Use the [MODIFIER] push-buttons to modify the present setting of the phase offset. Observe that the oscilloscope and note that a phase offset is generated.
4. Depress the [P.SET] to restore phase offset to factory default phase offset value (0°).

3-13-3-2. Using Model 8550 as a Frequency Counter

Model 8550 employs a built-in frequency counter circuit which is used in different parts of the instrument for various purposes. This internal counter is utilized when the instrument is placed in its PLL operating mode for automatic detection of the frequency of the external reference. The frequency counter reading is made available to the user and can measure external frequencies from 10Hz to over 60MHz. Frequency reading is given with fixed resolution of 4 digits. Decimal point and exponent are displayed automatically. To use Model 8550 as a frequency counter proceed as follows:

1. Depress the [POWER] switch once to turn the power on.
2. Depress the operating mode push-buttons until the light behind PLL illuminates.
3. Modify trigger level parameter (TRIG LEVEL) to the required thrash-hold level.
4. Remove any BNC cable from front panel connectors.
5. Depress the [FUNC] push-button in the MAIN PARAMETERS group until the light behind FREQ illuminates; observe the programmed frequency setting.
5. Connect a BNC cable from the reference source to the front panel REF INPUT connector.
6. Observe that the displayed reading is modified to read the frequency of the external frequency and that the decimal point blinks at a constant rate; indicating that the display reads the frequency of the external signal.
7. Remove the BNC cable from the REF input connector and observe that the decimal point stopped blinking and that the display resumes its normal programmed frequency parameter.

3-13A. SELECTING AN OPERATING MODE - MODEL 8551

Model 8551 may operate as a normal function generator, as a variable pulse width pulse generator, as a fixed duty cycle pulse generator, and as a phase locking generator. Similar to Model 8550, selecting an operating modes is done by depressing one of the OPERATING MODE [⇑ or ⇓] push-buttons until the light behind the desired mode illuminates.

Description of the various modes which can be used on Model 8551 is given in the following.

3-13A-1. Normal Function Generator Operating Mode - Model 8551

Function generator operating mode is the normal operating conditions where the output waveform is symmetrical about its horizontal and vertical axis. The normal operating mode also permits a vertical offset of its output waveform. The generator is placed in its normal operating mode when the light behind FUNC illuminates. Triggered operation and externally controlled modes such as VCO and AM may operate in conjunction with the normal function generator operating mode.

3-13A-2. Pulse Generator With Variable Pulse Width Operating Mode - Model 8551

Model 8551 offers additional capability to the basic normal function generator by allowing modification of parameters which are associated with the pulse output. When the pulse generator operating mode is selected, one can modify the pulse width, the pulse period, and independently adjust the rise and the fall times. Variable ramp width function is also made available.

The generator is placed in its pulse generator operating mode when the light behind PULSE illuminates. Triggered operation and externally controlled modes such as PWM, VCO, and AM may operate in conjunction with the pulse generator operating mode. Access to the DUTY parameter is automatically inhibited by the generator.

3-13A-3. Pulse Generator With Fixed Duty Cycle Operating Mode - Model 8551

Some applications require that the ratio between the pulse width to the pulse period remain constant regardless of the programmed period. The pulse generator with fixed duty cycle operating mode is a special case of the normal pulse generator which provides control over the duty cycle rather than the pulse width. In this mode, the user should only program the required duty cycle. Then, while changing

the period, the instrument automatically adjusts the duty cycle ratio at the output connector.

The duty cycle may be selected within the range of 1% to 8550%, however, this range may be extended to almost 99% by using the pulse complement function.

The generator is placed in its fixed duty cycle operating mode when the light behind F.DTY illuminates. Triggered operation and externally controlled modes such as PWM, VCO, and AM may operate in conjunction with the pulse generator operating mode. Access to the WIDTH parameter is automatically inhibited by the generator.

3-13A-4. Phase Locking Generator Operating Mode - Model 8551

Model 8551 employs an automatic locking circuit which enables phase and frequency locking to an external reference. Model 8551 locks on the external reference signal regardless of its programmed frequency setting. After the generator has locked on the signal, the user may generate a phase offset between the external signal and the signal at the output connector. Offset range is ±180°.

The generator is placed in its phase locking operating mode when the light behind PLL illuminates. The phase locking operating mode can not be operated in conjunction with the triggered modes. To operate the instrument in its PLL operating mode proceed as follows:

1. Depress the [POWER] switch once to turn the power on.

2. Depress the operating mode push-buttons until the light behind PLL illuminates.

3. Modify trigger level parameter (TRIG LEVEL) to the required thrash-hold level.

4. Connect a BNC cable from the reference source to the front panel REF INPUT connector. Use a “T” connector and connect the reference signal to channel A on an oscilloscope.

5. Connect a BNC cable from 8551 output to channel B on the oscilloscope.

6. Set oscilloscope and observe that the two signals have the same frequency and are locked on the same phase.

3-13A-4-1. Generating Phase Offsets

As discussed in paragraph 3-12A-4, the generator is capable of generating phase offsets between the external reference signal and the main output connector. To generate phase offset proceed as follows:

1. Repeat the operating instruction as in the previous paragraph.
2. Depress the [FUNCTION] push-button until the light behind PHASE illuminates.
3. Use the [MODIFIER] push-buttons to modify the present setting of the phase offset. Observe that the oscilloscope and note that a phase offset is generated.
4. Depress the [P.SET] to restore phase offset to factory default phase offset value (0°).

3-13A-4-2. Using Model 8551 as a Counter/Timer

Model 8551 employs a built-in counter/timer circuit which is used in different parts of the instrument for various purposes. This internal counter/timer is utilized when the instrument is placed in its PLL operating mode for automatic detection of the frequency of the external reference.

The counter/timer reading is made available to the user and can measure external frequencies from 10Hz to over 60MHz and external periods from .1s to 16ns. Frequency and period readings are given with fixed resolution of 4 digits. Decimal point and exponent are displayed automatically.

To use Model 8551 as a frequency counter proceed as follows:

1. Depress the [POWER] switch once to turn the power on.

2. Depress the operating mode push-buttons until the light behind PLL illuminates.

3. Modify trigger level parameter (TRIG LEVEL) to the required threshold level.

4. Remove any BNC cable from front panel connectors.

5. Depress the [FUNC] push-button in the MAIN PARAMETERS group until the light behind FREQ illuminates; observe the programmed frequency setting.

5. Connect a BNC cable from the reference source to the front panel REF INPUT connector.

6. Observe that the displayed reading is modified to read the frequency of the external signal and that the decimal point blinks at a constant rate; indicating that the generator is its timer mode of operation.

7. Remove the BNC cable from the REF input connector and observe that the decimal point stopped blinking and that the display resumes its normal programmed frequency parameter.

To use Model 8551 as a timer proceed as follows:

1. Depress the [POWER] switch once to turn the power on.

2. Depress the operating mode push-buttons until the light behind PLL illuminates.

3. Modify trigger level parameter (TRIG LEVEL) to the required thrash-hold level.

4. Remove any BNC cable from front panel connectors.

5. Depress the [PULSE] push-button in the MAIN PARAMETERS group until the light behind PER illuminates; observe the programmed period setting.

6. Connect a BNC cable from the reference source to the front panel REF INPUT connector.

7. Observe that the displayed reading is modified to read the period of the external signal and that the decimal point blinks at a constant rate; indicating that the generator is its timer mode of operation.

8. Remove the BNC cable from the REF input connector and observe that the decimal point stopped blinking and that the display resumes its normal programmed period parameter.

3-14. SELECTING A MODULATION MODE

Model 8550 provides three modulation modes: FM, AM, and VCO. Model 8551 offers PWM, AM, and VCO. Placing the instrument in one of these modulation modes is done by depressing the push-buttons in the MOD section until the light nest to the required modulation mode. The controlling signal is applied to the front panel INPUT BNC connector.

3-14-1. Frequency Modulation (FM) Mode (Model 8550 only)

The generator, when placed in this mode, operates as a free running voltage controlled oscillator. The applied sinewave at the MOD INPUT connector determines modulation characteristics. Model 8550 is placed in its FM mode when the light behind FM illuminates.

To frequency modulate the instrument first select the FM control mode, and then apply the modulating signal to the front panel INPUT connector. Observe external signal limits to avoid damage to the input circuit.

3-14-2. Amplitude Modulation (AM) Mode

The instrument, when placed in this mode, releases its amplitude control to an external control. A signal with an appropriate characteristics modulates the amplitude at the main output connector. Any of the available output waveforms may be modulated by the AM input modulating signal. Model 8550 is placed in its AM mode when the light behind AM illuminates.

To amplitude modulate the generator first select the AM control mode, and then apply the modulating signal to the front panel INPUT connector. Frequency and amplitude limits of the modulating signal should be observed to avoid damage to the input circuit.

3-14-3. Voltage Controlled Oscillator (VCO) Mode

Placing the function generator in VCO (voltage controlled oscillator) operating mode removes the frequency control from its output connector. The frequency of the selected waveform is then proportional to an amplitude level of a signal which may be applied to the VCO IN connector. The instrument is placed in its VCO mode when the light behind VCO illuminates.

To operate the generator as a voltage controlled amplifier first select the VCO mode, then apply the control voltage to the front panel INPUT connector. Input limits should be observed to avoid damage to the input circuit. Note that, although the FM mode is not available on the Model 8551, if required, the VCO input may be used to frequency modulate the generator.

3-14-4. Pulse Width Modulation (PWM) Mode (model 8551 only)

Placing the Model 8551 in PWM (pulse width modulation) operating mode removes the pulse width control from its output connector. The pulse width at the output connector is then proportional to an amplitude level of a signal which is applied to the front panel control input. The instrument is placed in its PWM mode when the light behind PWM illuminates.

To pulse width modulate the generator first select the PWM mode, then apply the control signal to the front panel INPUT connector. Input limits should be observed to avoid damage to the input circuit.

3-15. SELECTING AN OUTPUT WAVEFORM

Selecting one of the available output waveforms is done by depressing one of the two push-buttons in the OUTPUT section until the light behind the required

waveform illuminates. Model 8550 makes available six different waveforms through the OUTPUT connector. These waveforms are:

SINE WAVE	**POSITIVE SQUARE WAVE**
TRIANGLE	**NEGATIVE SQUARE WAVE**
DC	**SQUARE WAVE**

Model 8551 offers eight additional waveforms (DC output function is omitted):

PULSE
PULSE COMPLEMENT
POSITIVE PULSE
POSITIVE PULSE COMPLEMENT
NEGATIVE PULSE
NEGATIVE PULSE COMPLEMENT
RAMP
INVERTED RAMP

Note that pulse complements are selected using the 2nd function selection procedure. For more information on operating 2nd functions refer to paragraph 3-9.

3-16. DISABLING THE OUTPUT

The Model 8550/8551 features a stand-by mode which disconnects the signal from the output connectors. The stand-by function is especially useful in automatic test systems where the output is constantly connected to the device under test and where modification of waveform parameters may endanger this device. Note that after power up or software reset, the output is disabled.

To resume normal operation simply depress one of the push-button in the OUTPUT section. The light behind the previously selected waveform illuminates; indicating that the output signal in now connected to the output connector.

To place the instrument in its stand-by mode depress in sequence the [2nd] and the [ST-BY] push-buttons. The selected waveform light turns off; indicating that the output signal is disconnected from the output connector.

3-17. TRIGGERING THE FUNCTION GENERATOR

Model 8550/8551 when set to one of its trigger modes accepts stimulation from a variety of sources. The Operator has the option of selecting either an external source, an internal source, or a manual source. Each triggering method is used in a different way and for different applications. The triggering options are described in the following.

3-17-1. Triggering The Function Generator With An External Stimulant

Selecting one of the external triggering modes is simply a matter of depressing push-buttons in the TRIGGER section until the light behind the desired mode illuminates. When no light in the TRIGGER MODE section is on, the function generator operates in its normal continuous mode.

The Model 8550/8551 triggers on the leading edge of the applied external signal. The internal trigger level is programmable within the range of ±10V. The instrument may operate in one of the following external triggering modes: Triggered, Gated, or in Counted burst mode. Each mode is described in the following.

3-17-1-1. Triggered Mode

When set to operate in triggered mode, each positive going transition at the TRIG/REF INPUT connector generates a single waveform at the OUTPUT connector. The waveform at the output connector is automatically synchronized with the external transition. To trigger the generator from an external source proceed as follows:

1. Depress the [POWER] switch once to turn the power on.
2. Select the required output waveform and set up the parameters to the required characteristics.
3. Modify trigger level parameter (TRIG LEVEL) to the required thrash-hold level.
4. Depress the TRIGGER MODE push-button until the light behind TRIG'D illuminates.
5. Connect a BNC cable from the external stimulant to the front panel TRIG/REF INPUT connector. Make sure to observe external signal limits to avoid damage to the input circuit.
6. When done with the triggered operation remove the BNC cable from the input connector and select the normal continuous mode.

3-17-1-2. Gated Mode

When set to operate in gated mode, the first positive going transition at the TRIG/REF INPUT connector enables the generator output. The consecutive negative going transition disables the generator output. First output waveform is synchronized with the first external transition. Last waveform is always completed.

NOTE

The TRIG/REF INPUT connector is sensitive to dc levels. If this input is left open and the trigger level was set to a negative voltage, the generator may self gate.

To gate the generator from an external source proceed as follows:

1. Depress the [POWER] switch once to turn the power on.

2. Select the required output waveform and set up the parameters to the required characteristics.

3. Modify trigger level parameter (TRIG LEVEL) to the required thrash-hold level.

4. Depress the TRIGGER MODE push-button until the light behind GATED illuminates.

5. Connect a BNC cable from the external stimulant to the front panel TRIG/REF INPUT connector. Make sure to observe external signal limits to avoid damage to the input circuit.

6. When done with the gated operation remove the BNC cable from the input connector and select the normal continuous mode.

3-17-1-3. Counted Burst Mode

When set to operate in counted burst mode, each positive going transition at the TRIG/REF INPUT connector generates a train of waveforms at the OUTPUT connector. The number of generated waveforms are programmable within the range of 1 to 4000. The first waveform at the output connector is automatically synchronized with the external transition.

To generate a counted burst using an external source proceed as follows:

1. Depress the [POWER] switch once to turn the power on.

2. Select the required output waveform and set up the parameters to the required characteristics.

3. Modify trigger level parameter (TRIG LEVEL) to the required thrash-hold level.

4. Depress the TRIG push-button in the MAIN PARAMETERS group until the light behind BUR illuminates. Modify the burst parameter to the required count.

5. Depress the TRIGGER MODE push-button until the light behind BURST illuminates.

6. Connect a BNC cable from the external stimulant to the front panel TRIG/REF INPUT connector. Make sure to observe external signal limits to avoid damage to the input circuit.

7. When done with the counted burst operation remove the BNC cable from the input connector and select the normal continuous mode.

3-17-2. Triggering The Function Generator With An Internal Stimulant

When an external source is not available, the operator has the option of using the built-in trigger stimulant. The internal trigger generator is a free running generator, asynchronous to the main output generator, with a programmable period. Signal applied to the TRIG/REF INPUT will have no effect on the generator when it is placed in internal trigger mode. The internal trigger may be used in conjunction with the triggered and the counted burst modes; it can not, however, be used in gated mode. Operating the internal trigger generator in triggered and counted burst modes is described in the following.

3-17-2-1. Triggered Mode

When set to operate in internal triggered mode, the output connector generates one waveform at programmable intervals. Note that the programmed internal period should not exceed one half of the output waveform duration otherwise an error will result (Model 8551 will indicate such errors with an ERROR LED). To trigger the generator from the internal trigger generator proceed as follows:

1. Depress the [POWER] switch once to turn the power on.

2. Select the required output waveform and set up the output parameters to the required characteristics.

3. Modify internal trigger period (PER) to the required interval.

4. Depress the TRIGGER MODE push-button until the light behind TRIG'D illuminates.

5. Depress [2nd] and then the [MAN] push-buttons and observe that the I.TRG light illuminates; indicating that the internal trigger stimulant is now active.

3-17-2-2. Counted Burst Mode

When set to operate in internal counted burst mode, the output connector generates a train of counted waveforms at programmable intervals. Note that the programmed internal period should not exceed the period of the complete burst duration otherwise an

error will result (Model 8551 will indicate such errors with an ERROR LED). To generate a counted burst using the internal period generator proceed exactly as described in paragraph 3-17-2-1, except select the BURST mode.

3-17-3. Triggering The Function Generator With A Manual Stimulant

The MAN button simulates an external signal. If the generator is placed in GATED mode, an output signal will be available as long as the MAN push-button is depressed. When the generator is set to TRIG'D (triggered) mode, each time the MAN button is depressed a single output waveform is generated. When the Model 8550/8551 is set to generate a counted burst, each time the MAN push-button is depressed the output generates a train of counted waveforms at programmable intervals. The MAN push-button has no effect in normal mode of operation or when the instrument is set to internal trigger mode.

3-18. USING THE OFFSET

The function generator employs two level windows; allowing amplitude and offset to be independently selected within these levels. When setting up the offset parameter, one must keep in mind that the offset is attenuated with the signal. The user has no control over the selected internal amplitude range. This may cause some confusion since not knowing this fact may produce an offset error at an amplitude-offset combination that seems to be reasonable. It is therefore suggested to first set up the amplitude parameter and only then to set the required offset level. An attempt to modify the offset parameter beyond the capability of the instrument will generate an error indication. Offsets and amplitudes are independently selectable within the level windows given in Table 3-3.

3-19. USING FRONT PANEL SET-UPS

Setting-up all parameters in a versatile instrument such as the Model 8550/8551 takes some time. The set-up time is longer when a number of tests are performed and more than one set-up is required. The function generator incorporates a non-volatile memory that preserves stored information for a long time. The size of the non-volatile memory permits storage of up to 30 complete front panel set-ups. Front panel set-ups can be recalled one at a time. The generator also employs a special recall mode that permits automatic scrolling through the stored set-ups for sequential tests. The operator may select to scroll in an ascending or descending order. Description how to save and recall set-ups and how to use the recall mode is given in the following.

3-19-1. Storing Set-ups

First modify front panel parameters as necessary to perform the required test. Parameter modification procedure is discussed in paragraph 3-12. When all parameters are programmed and verified for accuracy, proceed with storing this set-up as follows:

1. Depress the [2nd] and [STORE] push-button in sequence and observe that the display is modified to indicate the following:

S xx ?
"?" appears blinking

"S" means that the instrument is placed in memory store mode. "xx" indicates the number of the present storage cell. Numbers may range from 00 to 30. Depressing any other push-button removes the generator from the memory store mode and leaves front panel settings unchanged.

2. To program individual memory cells for a specific front panel set-up depress the MODIFIER [x1 ⇑] or [x1 ⇓] until the desired memory number is displayed. Depressing [EXE] locks in the entire front panel set-up for later usage. The instrument then resumes normal operation.

3. Repeat the above procedure for as many set-ups that are required. Stored front panel set-ups are limited to 30.

3-19-2. Recalling Set-ups

Level Window	Amplitude Range	Offset Range
±8.00V	100mV to 16.0V	0V to ±7.95V
±800mV	10mV to 99.9mV	0V to ±795mV

Tabel 3-3. Offset-Amplitude Programming Limits

The Model 8550/8551 employs a non-volatile memory (RAM). The computer circuit continuously monitors front panel traffic and saves it in a special location within the RAM. This location is separated from the stored front panel set-ups. After turning AC MAINS off or in case of an accidental power failure, the generator updates front panel indicators with the last set-up before power shut-down. To recall a stored front panel set-up proceed as follows:

1. Depress the [2nd] and [RECALL] push-button in sequence and observe that the display is modified to indicate the following:

C xx ?
"?" appears blinking

"C" means that the instrument is placed in memory recall mode. "xx" indicates the number of the present storage cell. Numbers may range from 00 to 30. Depressing any other push-button removes the generator from the memory recall mode and leaves front panel settings unchanged.

2. Recalling a specific front panel set-up is done by depressing the MODIFIER [x1 ⇑] or [x1 ⇓] until the desired cell number is displayed. Depressing [EXE] updates front panel set-up with the parameters which were stored in the selected memory cell.

3. Repeat the above procedure for as many set-ups that are required. Recalled front panel set-ups are limited to 30.

3-19-2-1. Using The Recall Mode

Model 8550/8551 employs a special recall mode which permits ascended or descended scroll through a number of set-ups by pressing either the MODIFIER [x1 ⇑] or [x1 ⇓] push-buttons respectively. This mode is especially useful for repetitive procedures such as calibration and performance tests.

To set the function generator for operation in its recall mode proceed as follows:

1. Depress the [2nd] push-button and observe that the display is modified to indicate the following:

2nd ?
? appears flashing

2. Depress the [RCL MODE] push-button and observe that the display is modified to indicate the following:

C 00 ?

The instrument is now set to operate in its recall mode. The display is first updated with the parameters which were stored in memory cell 00.

3. Use the MODIFIER [x1 ⇑] or [x1 ⇓] to scroll through the memory bank.

4. Depress any other front panel push-button to exit this function and to return to normal display operation.

3-20. CHANGING THE GPIB ADDRESS

GPIB address is modified using front panel programming. The GPIB address is stored in the non-volatile memory, therefore, conventional address switches are not provided. Detailed instructions how to change the GPIB address are given in Paragraph 4-7.

3-21. CHANGING EMULATION MODE TO HP

Models 8550 and 8551 can be made fully compatible with HP Model 8116A device-dependent commands set. HP 8116A is a 50MHz function generator that provides similar functions to those offered in Models 8550 and 8551. The three instruments do not offer the same functions and feature, however, in places where they are the same, the GPIB commands that are used for programming these instruments are the same. This emulation mode saves extremely valuable programming time when replacing Model 8116A by Model 8550 or Model 8551.

The complete set of commands that are used with HP 8116A are listed in Table 4-8. Information on how to change Models 8550 and 8551 settings from normal GPIB programming to HP programming mode is given in paragraph 4-16.

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GPIB Operation Section 4

4-1. INTRODUCTION

The GPIB (general purpose interface bus) is an instrumentation data bus with standards originally adopted by the IEEE (Institute of Electrical and Electronic Engineering) in 1975 and given the IEEE-488 designation. In November 1987 the IEEE-488 document was revised, primarily for editorial classification and addendum, and the new document was identified as IEEE-488-1978.

This document has been the standard for general-purpose instrumentation bus (GPIB) which has been adopted by worldwide instrumentation manufacturers. In June 1987 the IEEE approved a new standard for programmable instruments and devices IEEE Standard 488.2-1987 Codes, Formats, Protocols, and Common Commands. The original document, IEEE-488-1978, was re-titled IEEE-488.1.

The IEEE-488.2 standard was designed to make the interface system easier to use by requiring that all devices provide certain capabilities such as talk and listen, respond to device clear commands, and be capable of service requests. Other functions such as parallel poll are left optional with the instrument manufacturer. The Model 8550 complies with all of the mandatory IEEE-488.1 and IEEE-488.2 requirements. Some of the issues which IEEE-488.2 Addresses are:

1. A required minimum set of IEEE-488.1 capabilities.
2. Reliable transfer of messages between a talker and listener and precise syntax in those messages.
3. A set of commands which would be useful in all instruments.
4. Common serial poll status reporting.
5. Synchronization programming with instrument functions.

This section contains general bus information as well as detailed programming information and is divided as follows:

1. General introductory information pertaining to the IEEE-488 bus may be found primarily in paragraphs 4-2 through 4-5.
2. Information necessary to connect the Model 8550 to the bus and to change the bus address is contained in paragraphs 4-6 and 4-7.
3. Programming of the instrument with general bus command is covered in paragraph 4-8.
4. Device-dependent command programming is described in detail in paragraph 4-10. The commands outlined in this section can be considered to be the most important since they control virtually all instrument functions.
5. Additional information pertaining to device status reporting and error messages can be found in paragraphs 4-13 and 4-15.

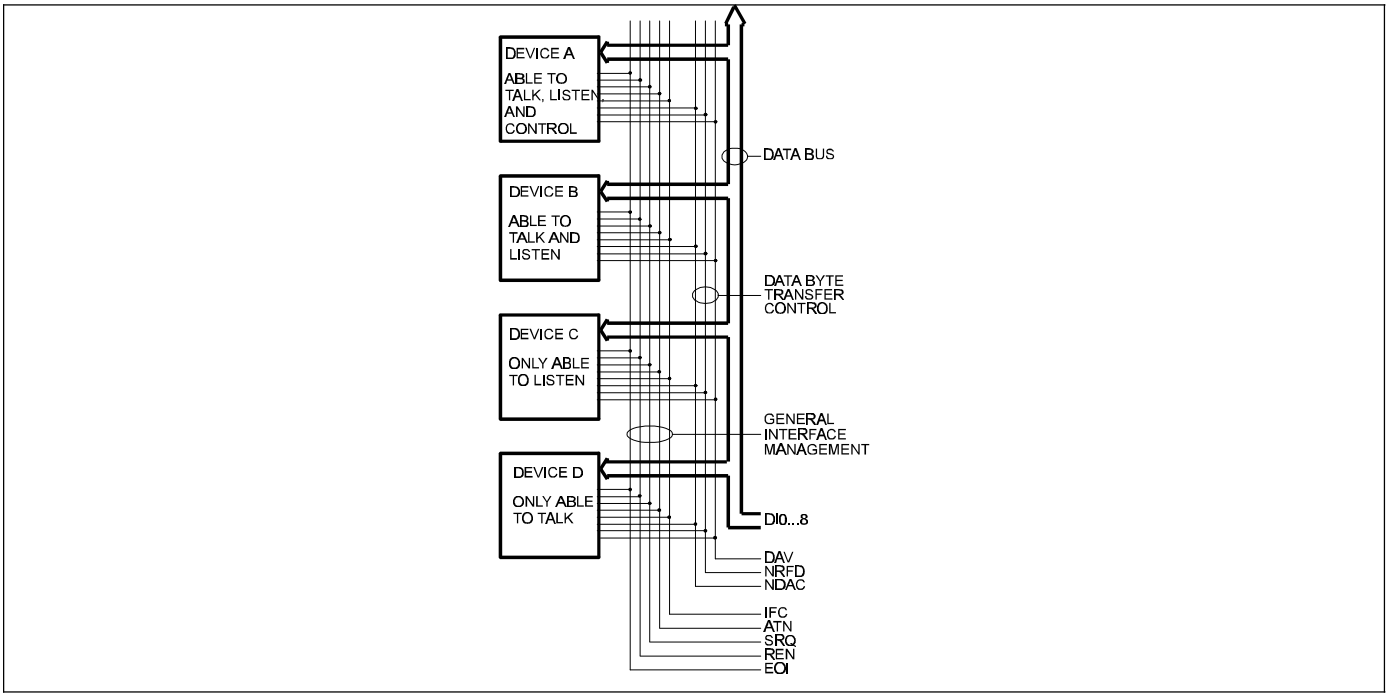
4-2. BUS DESCRIPTION

The IEEE-488 bus was designed as a parallel data transfer medium to optimize data transfer without using as excessive number of bus lines. In keeping with this goal, the bus has only eight data lines which are used for both data and most commands. Five bus management lines and three handshake lines round out the complement of signal lines. Since the bus is of parallel design, all devices connected to the bus have the same information available simultaneously. Exactly what is done with the information by each device depends on many factors, including device capabilities.

A typical bus configuration for remote controlled operation is shown in Figure 4-1. The typical system will have one controller and one or more instruments to which commands are given and from which data is received. There are three categories that describe device operation. These include: controller; talker; listener.

The controller controls other devices on the bus. A talker sends data, while a listener receives data. an instrument, may be a talker only, a listener only, or both a talker and listener.

Figure 4-1. IEEE Bus Configuration



Any given system can have only one controller (control may be passed to an appropriate device through a special command). Any number of talkers or listeners may be present up to the hardware constraints of the bus. The bus is limited to 15 devices, but this number may be reduced if higher than normal data transfer rates are required or if long interconnect cables are used.

Several devices may be commanded to listen at once, but only one device may be a talker at any given time. Otherwise, communications would be scrambled much like an individual is trying to select a single conversation out of a large crowd.

Before a device can talk or listen, it must be appropriately addressed. Devices are selected on the basis of their primary address. The addressed device is sent a talk or listen command derived from its primary address. Normally, each device on the bus has a unique primary address so that each may be addressed individually. The bus also has another addressing mode called secondary addressing, but not all devices use this addressing mode.

Once the device is addressed to talk or listen, appropriate bus transactions may be initiated. For example, if an instrument is addressed to talk, it will usually place its data on the bus one byte at a time. The listening device will then read this information, and the appropriate software is then be used to channel the information to the desired location.

4-3. IEEE-488 BUS LINES

The signal lines on the IEEE-488 bus are grouped into three general categories. The data lines handle bus information, while the handshake and bus management lines assure that proper data transfer and bus operation takes place. Each of the bus lines is “active low” so that approximately zero volts is a logic “one”. The following paragraphs describe the purpose of these lines, which are shown in Figure 4-1.

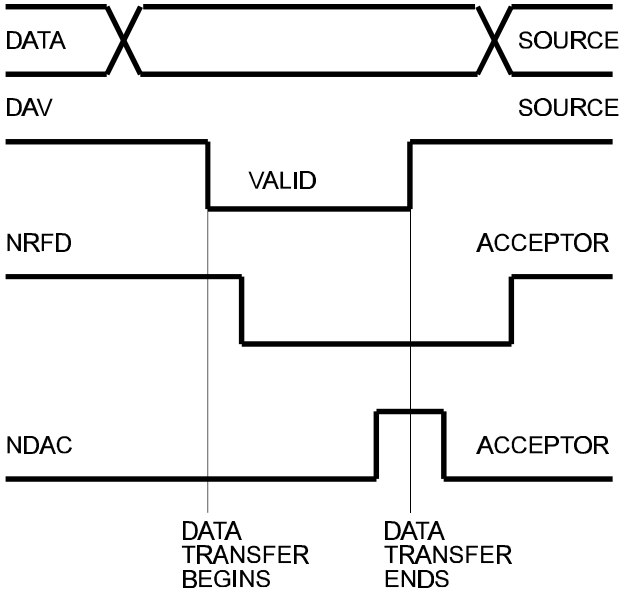
4-3-1. Bus Management Lines

The bus management group is made up of five signal lines that provide orderly transfer of data. These lines are used to send the uniline commands described in paragraph 4-8-1.

1. ATN (Attention) - the ATN line is one of the more important management lines. The state of the ATN line determines whether controller information on the data bus is to be considered data or a multiline command as described in paragraph 4-8-2.

2. IFC (Interface Clear) - Setting the IFC line true (low) causes the bus to go to a known state.

Figure 4-2. IEEE Handshake Sequence



3. REN (Remote Enable) - Setting the REM line low sends the REM command. This sets up instruments on the bus for remote operation.

4. EOI (End Or Identify) - The EOI line is used to send the EOI command that usually terminates a multi-byte transfer sequence.

5. SRQ (Service Request) - the SRQ line is set low by a device when it requires service from the controller.

4-3-2. Handshake Lines

The bus uses three handshake lines that operate in an interlocked sequence. This method assures reliable data transfer regardless of the transfer rate. Generally, data transfer will occur at a rate determined by the slowest active device on the bus.

One of the handshake lines is controlled by the data source, while the remaining two lines are controlled by accepting devices. The three bus handshake lines are:

1. DAV (Data Valid) - The source controls the state of the DAV line.

2. NRFD (Not Ready For Data) - the acceptor controls the state of the NRFD line.

3. NDAC (Not Data Accepted) - the acceptor also controls the NDAC line.

The complete handshake sequence for one data byte is shown in Figure 4-2. Once data is on the bus, the source checks to see that NRFD is high, indicating that all devices on the bus are ready for data. At the same time NDAC should be low from the previous byte transfer. If these conditions are not met, the source must then wait until the NRFD and NDAC lines have the correct status. If the source is controller, NRFD and NDAC must remain stable for at least 100 ns after ATN is set low. Because of the possibility of bus hang up, some controllers have time-out routines to display error messages if the handshake sequence stops for any reason.

Once the NRFD and NDAC lines are properly set, the source sets the DAV line low, indicating that data on the bus is now valid. the NRFD line then goes low; the NDAC line goes high once all devices on the bus have accepted the data. Each device will release the NDAC line at its own rate, but the NDAC line will not go high until the slowest device has accepted the data byte.

After the NDAC line goes high, the source then sets the DAV line high to indicate that the data on the bus is no longer valid. At this point, the NDAC line returns to its low state. Finally, the NRFD line is released by each of the devices at their own

rates, until the NRFD line finally goes high when the slowest device is ready, and the bus is set to repeat the sequence with the next data byte.

The sequence just described is used to transfer both data and multiline command. The state of the ATN line determines whether the data bus contains data or commands.

4-3-3. Data Lines

The IEEE-488.2 bus uses the eight data lines that allow data to be transmitted and received in a bit-parallel, byte-serial manner. These eight lines use the convention DI01 through DI08 instead of the more common D0 through D7 binary terminology. The data lines are bi-directional and, as with the remaining bus signal lines, low is true.

4-4. INTERFACE FUNCTION CODES

The interface function codes are part of the IEEE-488.2 standards. These codes define an instrument's ability to support various interface functions and should not be confused with programming commands found elsewhere in this manual.

Table 4-1 lists the codes for the Model 8550. The numeric value following each one or two letter code define Model 8550 capability as follows:

SH - (Source Handshake Function) - The ability for the Model 8550 to initiate the transfer of message/data on the data bus provided by the SH function.

AH - (Acceptor Handshake Function) - The ability for the Model 8550 to guarantee proper reception of message/data on the data bus provided by the AH function.

T - (Talker Function) - The ability of the Model 8550 to send device-dependent data over the bus (to another device) is provided by the T function. Model 8550 talker capabilities exist only after the instrument has been addressed to talk.

L - (Listen Function) - The ability of the Model 8550 to receive device-dependent data over the bus (from anther device) is provided by the L function. Listener function capability of the Model 8550 exist only after it has been addressed to listen.

RS - (Service Request Function) - The ability of the Model 8550 to request service from the controller is provided by the RS function.

RL - (Remote-Local Function) - The ability of the Model 8550 to be placed in remote or local modes is provided by the RL function.

Table 4-1. Model 8550 Interface Function Codes

CODE	INTERFACE FUNCTION
SH1	Source Handshake Function
AH1	Acceptor Handshake Capabilities
T6	Talker (basic talker, serial poll, unaddressed to talk on LAG)
L4	Listener (basic listener, unaddressed to listen on TAG)
SR1	Service request capability
RL1	Remote/Local capability
PP2	Parallel Poll capability
DC1	Device Clear capability
DT1	Device Trigger capability
C0	No controller capability
E1	Open collector bus drivers
TE0	No Extended Talker capabilities
LE0	No Extended Listener capabilities

PP - (parallel Poll Function) - The ability of the Model 8550 to respond to a parallel poll request from the controller is provided by the PP function.

DC - (Device Clear Function) - The ability for the Model 8550 to be cleared (initialized) is provided by the DC function.

DT - (Device Trigger Function) - The ability of the Model 8550 to have its output triggered is provided by the DT function.

C - (controller Function) - The Model 8550 does not have a controller function.

TE - (Extended Talker Capabilities) - The Model 8550 does not have extended talker capabilities.

LE - (Extended Listener Function) - The Model 8550 does not have extended listener function.

4-5. SOFTWARE CONSIDERATIONS

The most sophisticated computer in the world would be useless without the necessary software. This basic requirement is also true of the IEEE-488.2 bus, which requires the use of handler routines as described in this paragraph. Before a controller can be used with the IEEE-488.2 interface, the user must make certain that appropriate handler software is present within the controller. With the IBM PC computer, for example, the GPIB interface card must be used with an additional software which contains the necessary handler software.

Other small computers that can be used as controllers have limited IEEE command capability. The capabilities of some computers depends on the particular interface being used. Often, little software "tricks" are required to achieve the desired results.

From the preceding discussion, the message is clear: make sure the proper software is being used with the instrument. Often, the user may incorrectly suspect that a hardware problem is causing fault, when it was the software that was causing the problem all along.

4-6. HARDWARE CONSIDERATIONS

Before the instrument can be used with the IEEE-488 bus, it must be connected to the bus with a suitable connector. Also, the primary address must be properly programmed as described in this section.

4-6-1. Typical Controlled Systems

The IEEE-488.2 bus is a parallel interface system. As a result, adding more devices is simply a matter of using more cables to make the desired connections. Because of this flexibility, system complexity can range from simple to extremely complex.

The simplest possible controlled system comprises a controller and one Model 8550. The controller is used to send commands to the instrument, which sends data back to the controller.

The system becomes more complex when additional instruments are added. Depending on programming, all data may be routed through the controller, or it may be transmitted directly from one instrument to another.

4-6-2. Connections

The instrument is connected to the bus through an IEEE-488.2 connector. This connector is designed to be stacked to allow a number of parallel connections on one instrument.

NOTE

To avoid possible mechanical damage, it is recommended that no more than three connectors be stacked on any one instrument. Otherwise, the resulting strain may cause internal damage to the connectors.

The IEEE-488.2 bus is limited to a maximum of 15 devices, including the controller. Also, the maximum cable length is 20 meters. Failure to observe these limits will probably result in erratic bus operation.

Custom cables may be constructed using the information in Table 4-2. Table 4-2 also lists the contact assignments for the various bus lines.

Table 4-2. IEEE-488 Contact Designations

Contact Number	IEEE-488 Designation	Type
1	DIO1	Data
2	DIO2	Data
3	DIO3	Data
4	DIO4	Data
5	EOI	Management
6	DAV	Handshake
7	NRFD	Handshake
8	NDAC	Handshake
9	IFC	Management
10	SRQ	Management
11	ATN	Management
12	SHIELD	Ground
13	DIO5	Data
14	DIO6	Data
15	DIO7	Data
16	DIO8	Data
17	REN	Management
18-24	Gnd	Ground

Contacts 18 through 24 are return lines for the indicated signal lines, and the cable shield is connected to contact 12. Each ground line is connected to digital common in the Model 8550.

CAUTION

The voltage between IEEE common and ground must not exceed 0 V or damage may result to your instrument.

4-7. CHANGING GPIB ADDRESS

The primary address of your instrument may be programmed to any value between 0 and 30 as long as the selected address is different from other devices addresses in the system. This may be accomplished using a front panel programming sequence. Note that the primary address of the instrument must agree with the address specified in the controller's program.

NOTE

The programmed primary address is briefly displayed during the power-up cycle of the Model 8550. It is stored in the non-volatile memory of the

instrument and is retained even when power is turned off.

To check the present address, or to enter a new one, proceed as follows:

1. Depress the [2nd] push-button once then depress the [GPIB ADR] push-button. The display will be modified to display the following:

GPxx

Where x may be any number from 0 to 30.

2. Use the MODIFIER [x1⇑] or the [x1 ⇓] push-buttons for selecting a new GPIB primary address.

3. To store the newly selected primary address depress [EXE]. The instrument then resumes normal operation.

4-8. BUS COMMANDS

While the hardware aspect of the bus is essential, the interface would be essentially worthless without appropriate commands to control the communications between the various instruments on the bus. This paragraph briefly describes the purpose of the bus commands, which are grouped into the following three categories:

1. Uniline commands: Sent by setting the associated bus line low (true).

2. Multiline commands: General bus commands which are sent over the data lines with the ATN line low (true).

3. Device-dependent commands: Special commands that depend on device configuration; sent over the data lines with ATN high (false).

4. Common commands and queries: A special set of commands that all devices must use and does not depend on device configuration; sent over the data lines in the same format as the device dependent commands.

4-8-1. Uniline Commands

Uniline commands are sent by setting the associated bus line to low. The ATN, IFC, and REN commands are asserted only by the system controller. The SRQ command is sent by an external device. The EOI command may be sent by either the controller or an external device depending on the direction of data transfer. The following is descriptions of each command.

REN - (Remote Enable) - The remote enable command is sent to the Model 8550 by the controller to set the instrument up for remote operation. Gen-

Table 4-3. IEEE-488 Bus Command Summary

COMMAND TYPE	COMMAND	STATE OF ATN LINE(*)	COMMENTS
Uniline	REN	X	Set up for remote operation
	EOI	X	Sent by setting EOI low
	IFC	X	Clears Interface
	ATN	Low	Defines data bus contents
	SRQ	X	Controlled by external device
Multiline Universal	LLO	Low	Locks out front panel controls
	DCL	Low	Returns device to default conditions
	SPE	Low	Enable serial polling
	SPD	Low	Disables serial polling Addressed
	SDC	Low	Returns unit to default condition
	GTL	Low	Returns to local control
	GET	Low	Triggers device for reading
Unaddress	UNL	Low	Removes all listeners from bus
	UNT	Low	Removes all talkers from bus
Device- Dependent(**)		High	Programs Model 8550 for various modes.

(*) X = Don't Care, (**) See paragraph 4-9 for complete description

erally, this should be done before attempting to program the instrument over the bus. The Model 8550 will indicate that it is in the remote mode by illuminating its front panel REM indicator. To place the Model 8550 in the remote mode, the controller must perform the following steps:

1. Set the REN line true.
2. Address the Model 8550 to listen.

NOTE

Setting REN true without addressing will not cause the REM indicator to turn on; however, once REN is true, the REM light will turn on the next time an address command is received.

EOI (End Or Identify) - The EOI command is used to positively identify the last byte in a multi-byte transfer sequence. This allows variable length data words to be transmitted easily.

IFC (Interface Clear) - The IFC command is sent to clear the bus and set hand shake lines to a known state. Although device configurations differ, the IFC command usually places instruments in the talk and listen idle states.

ATN (Attention) - The controller sends ATN while transmitting addresses or multiline commands. Device-dependent commands are sent with the ATN line high (false).

SRQ (Service Request) - The SRQ command is asserted by an external device when it requires service from the controller. If more than one device is present, a serial polling sequence, as described in paragraph 4-8-2, must be used to determine which has requested service.

4-8-2. Universal Multiline Commands

Universal commands are multiline commands that require no addressing. All instrumentation equipped to implement the command will do so simultaneously when the command is transmitted over the bus. As with all multiline commands, the universal commands are sent over the data lines with ATN set low:

LLO (Local Lockout) - The LLO command is sent by the controller to remove the Model 8550 from the local operating mode. Once the unit receives the LLO command, all its front panel controls (except Power) will be inoperative.

NOTE

The REN bus line must be true before the instrument will respond to an LLO command.

To lock out the front panel controls of the Model 8550, the controller must perform the following steps:

1. Set ATN true.
2. Send the LLO command to the instrument.

DCL (Device Clear) - The DCL command may be used to clear the Model 8550, setting it to a known state. Note that all devices on the bus equipped to respond to a DCL will do so simultaneously. When the Model 8550 receives a DCL command, it will return to the default conditions listed in Table 4-4. Factory pre-selected parameters are listed in Table 3-1. To send a DCL command the controller must perform the following steps:

1. Set ATN true.
2. Place the DCL command on the bus.

SPE (Serial Poll Enable) - The serial polling sequence is used to obtain the Model 8550 status byte. Usually, the serial polling sequence is used to determine which of several devices has requested service over the SRQ line. However, the serial polling sequence may be used at any time to obtain the status byte from the Model 8550. For more information on status byte format, refer to paragraph 4-14. The serial polling sequence is conducted as follows:

1. The controller sets the ATN line true.
2. The SPE (Serial Poll Enable) command is placed on the bus by the controller.
3. The Model 8550 is addressed to talk.
4. The controller sets ATN false.
5. The Model 8550 then places its status byte on the bus to be read by the controller.
6. The controller then sets the ATN line low and places SPD (Serial Poll Disable) on the bus to end the serial polling sequence.

Steps 3 trough 5 may be repeated for other instruments on the bus by using the correct talk address for each instrument. ATN must be true when the talk address is transmitted and false when the status byte is read.

SPD (Serial Poll Disable) - The SPD command is sent by the controller to remove all instrumentation on the bus from the serial poll mode.

Table 4-4. Default Conditions. (Status After SDC, DCL, or *RST)

AD = Mode	Default Status	
Operating Mode - Model 8550	F0	Normal
Sweep Direction	S1	Start to stop
Trigger Modes	M1	Normal continuous mode
Control Modes	CT0	Off
Output Waveforms	W1	Sinewave output
Output Disable/Enable Mode	D0	Output enabled
Pulse/Ramp Output Mode	C0	Complement OFF (Model 8551)
Edge Control	L0	Fastest edge transition (Model 8551)
Response Message Format	X0	Response header OFF
Response Message Terminator	Z0	New line(LF), END(EOI) terminator
Event Status Enable Mask	*ESE0	No mask
SRQ Enable Register Mask	*SRE0	No mask

4-8-3. Addressed Commands

Addressed commands are multiline commands that must be preceded by a listen command derived from the device's primary address before the instrument will respond. Only the addressed device will respond to each of these commands:

SDC (Selective Device Clear) - The SDC command performs essentially the same function as the DCL command except that only the addressed device will respond. This command is useful for clearing only a selected instrument instead of all devices simultaneously. Model 8550 will return to the default conditions listed in Tables 3-1 and 4-4 when responding to an SDC command. To transmit the SDC command, the controller must perform the following steps:

1. Set ATN true.
2. Address the Model 8550 to listen.
3. Place the SDC command on the data bus.

GTL (Go To Local) - The GTL command is used to remove the instrument from the remote mode of operation. Also, front panel control operation will usually be restored if the LLO command was previously sent. To send the GTL command, the controller must perform the following sequence:

1. Set ATN true.
2. Address the Model 8550 to listen.
3. Place the GTL command on the bus.

NOTE

The GTL command does not remove the local lockout state. With the local lockout condition previously set, the GTL command will enable front panel control operation until the next time a listener address command is received. This places the Model 8550 in the local lockout state again.

GET (Group Execute Trigger) - The GET command is used to trigger or arm devices to perform a specific task depends on device configuration. Although GET is considered to be an addressed command, many devices respond to GET without being addressed. Using the GET command is only one of several methods that can be used to initiate a trigger. More detailed information on triggering can be found in Section 3 of this manual. To send GET command over the bus, the controller must perform the following sequence:

1. Set ATN true.
2. Address the Model 8550 to listen.
3. Place the GET command on the data bus.

GET can also be sent without addressing by omitting step 2.

4-8-4. Unaddress Commands

The two unaddress commands are used by the controller to simultaneously remove all talkers and listeners from the bus. ATN is low when these multiline commands are asserted.

UNL (Unlisten) - All listeners are removed from the bus at once when the UNL commands is placed on the bus.

UNT (Untalk) - The controller sends the UNT command to clear the bus of any talkers.

4-8-5. Device-dependent Commands

The meaning of the device-dependent commands is determined by instrument configuration. Generally, these commands are sent as one or more ASCII characters that tell the device to perform a specific function. For example, M2 is sent to the Model 8550 to place the instrument in the external trigger mode. The IEEE-488.2 bus treats device-dependent commands as data in providing that ATN is high (false) when the commands are transmitted.

4-8-6. Common Commands and Queries

Since most instruments and devices in an ATE system use similar commands which perform identical functions, the IEEE-488.2 document has specified a common set of commands and queries which all device must use. This avoids the problem in which devices from various manufacturers used a different set of commands to enable functions and report status. The IEEE-488.2 treats the common commands and queries as device dependent commands. For example, *TRG is sent over the bus to trigger the instrument. Some common commands and queries, however, are optional; most of them are mandatory. The following set of command groups ensure that all devices communicate uniformly:

1. System Data - These commands are used to store or retrieve information such as device identification, descriptions and options. It is possible to determine the manufacturer, model, and serial number of the device under remote control.

2. Internal Operation - These commands include such instrument operations as resetting, self-calibrating, and self-diagnostics of a GPIB device. The device may respond to a calibration query to indicate that the calibration was carried out successfully and report any calibration errors that may have occurred. The reset command sets the device-dependent functions to a known state and must not affect the state of the IEEE-488 interface, the Service Request Enable register, or Standard Event Status Enable register.

3. Status and Event - These commands control the status structure of the GPIB device and provide a means to read and enable events. Included in these commands are Clear, Event Status Enable, Power-on Status, and Service Request Enable.

4. Synchronization - The operation of the devices within the system are synchronized with these commands. Included is a Wait to Continue command which forces the devices to complete all previous commands and queries. The Operation Complete command tells the device to set bit 0 in the Standard Event Status register when it completes all pending operations.

5. Device Trigger - These commands enable a device to be triggered and specify how it responds to the trigger message. The Define Device Trigger command stores a sequence of commands which the device will follow when the Group Execute Trigger (GET) is received.

6. Stored Settings - These commands are used to save the state of the device under control, to be used at a later time. The Save command stores the present state of the device in the device's memory. If there is more than one location in which this data can be stored, the command is followed by a number which designates the storage register to use. The Recall command restores the state of the device, as stored in its memory from the previous Save command. As with the Save command, the Recall command must be followed by a number to specify the register from which the stored settings are to be recalled.

4-9. DEVICE LISTENING FORMATS

This paragraph discusses the formatting of <Program Message> elements received by a device from its system interface. Allowable IEEE-488.2 <Program Message> is composed of sequence of <Program Message> units, each unit representing a program command. Each program command is composed of a sequence of functional syntactic elements. Legal IEEE-488.2 program commands are created from functional elements sequences.

Some commands of universal instrument system application have been defined by the IEEE-488.2. They are the common commands; these commands and queries are specific path selections through the functional syntax diagram as specified in the IEEE-488.2 standard. The remaining commands are device-specific and are generated by the device designer using the functional syntax diagram and the needs of the device. The functional elements include separators, terminators, headers, and data types. These elements are discussed in the following.

4-9-1. Functional Element Summary

<Program Message> Represents a sequence of zero or more <Program Message Unit> elements separated by <Program Message Unit Terminator> elements.

<Program Message Unit> Represents a single command or programming data received by the device.

<Command Message Unit> Represents a single command or programming data received by the device.

<Query Message Unit> Represents a single query sent from the controller to the device.

<Program Data> Represents any of the six different program data types.

<Program Message Unit separator> Separates the <Program Message Unit> elements from one another in a <Program Message>.

<Program Data Separator> Separates sequential <Program data> elements that are related to the same header.

<Program Header Separator> Separates the header from any associated <Program Data>.

<Program Message Terminator> Terminates a <Program Message>.

<Command Program Header> Specifies function operation. Used with any associated <Program Data elements>.

<Query Program Header> Similar to <Command Program Header> except a query indicator (?) shows that a response is expected from the device.

<Character Program Data> A data type suitable for sending short mnemonic data, generally where a numeric data type is not suitable.

<Decimal Numeric Program Data> A data type suitable for sending decimal integers or decimal fractions with or without exponents.

<Suffix Program Data> An optional field following <Decimal Numeric Program Data> used to indicate associated multipliers and units.

<NonDecimal Numeric Program Data> A data type suitable for sending integer numeric representation in base 16, 8, or 2. Useful for data that is more easily interpreted when directly expressed in a non-decimal format.

<String Program Data> A data type suitable for sending 7-bit ASCII character strings where the content needs to be “Hidden” (by delimiters)

<Arbitrary Block Program Data> A data type suitable for sending blocks of arbitrary 8-bit information.

<Expression Program data> A data type suitable for sending data that is elevated as one or more non-expression data elements before further parsing.

4-9-2. Separator Functional Element Summary

The various elements within the <Program Message> are separated by ASCII characters that were specially assigned for this purpose. These separators are discussed in the following paragraphs.

4-9-2-1. Program Message Unit Separator

The <Program Message Unit Separator> separates sequential <Program Message Unit> elements from one another within a <Program Message>. The <Program Message Unit Separator> is defined as:

;

It is allowed to use leading <white space> elements before the <Program Message Separator>. <White Space> is defined as a single ASCII-encoded byte in the range of 00-09, 0B-20. This range includes the ASCII control characters and the space, but excludes the new line.

4-9-2-2. Program Data Separator

The <Program Data Separator> separates sequential <Program Data> elements from one another after a <Command Program Header> or <Query Program Header>. It is used when a <Command Program Header> or <Query Program Header> has multiple parameters. The <Program Data Separator> is defined as:

,

Preceding and succeeding <White Space> elements are permitted.

4-9-2-3. Program Header Separator

The <Program Header Separator> separates the <Command Program Header> or <Query Program Header> from the <Program Data> elements. The <Program Header Separator> is defined as white space:

<White Space>

Refer to paragraph 4-9-2-1 for the definition of <White Space> elements.

4-9-3. Program Message Terminator

A <Program Message Terminator> terminates a sequence of one or more definite length <Program

Message Unit> elements. There are three possible <Program Message Terminator> elements:

1. NL (new line);
2. NL END (EOI); and
3. END (EOI)

NL is defined as a single ASCII-encoded byte 0A (10 decimal). Leading <White Space> elements are permitted. The instrument interprets any and all of the three terminators as semantically equivalent. No alternative encoding are allowed. Note that IEEE-P981 amendment forbids the use of CR as a <Program Message Terminator> element. This is because some controller treat CR as the end of transmission and leave the LF character in the unit, thereby creating an error in the controller.

4-9-4. Command Program Header

The <Command Program Header> represents the operation to be performed in a device. The header may be optionally followed by associated parameters encoded as <Program Data> elements. There are three defined <Command Program Header> elements: <Simple Command Program Header>, <Compound Command Program Header>, and <Common Command Program Header.

<Simple Command Program Header> is defined as:

<Program Mnemonic>

For example, FRQ. Leading <White Space> elements are permitted. Upper/lower case alpha characters are treated with the same semantic equivalence. <Compound Command Program Header> is not used in model 8550 and will not be discussed here. A <Common Command Program Header> is defined as:

***<Program Mnemonic>**

For example, *TRG. Leading <White Space> elements are permitted. Upper/ lower case alpha characters are treated with the same semantic equivalence.

4-9-5. Query Program Header

The <Query Program Header> represents the operation to be performed in a device. A <Query Program Header> causes the device to generate a response. This element may be optionally followed by associated parameters encoded as <Program Data> elements. There are three defined <Query Program Header> elements: <Simple Query Program Header>, <Compound Query Program Header>, and <Common Query Program Header. A <Simple Query Program Header> is defined as:

<Program Mnemonic>?

For example, FRQ?. Leading <White Space> elements are permitted. Upper/lower case alpha characters are treated with the same semantic equivalence. <Compound Query Program Header> is not used in model 8550 and will not be discussed here. A <Common Query Program Header> is defined as:

***<Program Mnemonic>?**

For example, *CAL?. Leading <White Space> elements are permitted. Upper/lower case alpha characters are treated with the same semantic equivalence.

4-9-6. Program Data

A <Program Data> functional element is used to convey a variety of parameter information related to the <Program Header>.

4-9-6-1. Character Program Data

The <Character Program Data> functional element is not implemented in Model 8550. Therefore it shall not be discussed in this manual.

4-9-6-2. Decimal Numeric Program Data

The <Decimal Numeric Program Data> is a flexible version of the three numeric representations as defined in ANSI X3.42-1975 - NR1, NR2, and NR3. A <Decimal Numeric Program Data> elements are defined as:

1. NR1 elements consists of a set of implicit point representations of numeric values. i.e. (+/-)12345.
2. NR2 elements are the representations of explicit point numeric values. i.e. (+/-)12.345.
3. NR3 elements are representations of scaled explicit radix point numeric values together with an exponent notation. i.e. (+/-)123.456E(+/-)3.

4-9-6-3. Suffix Program Data

A <Suffix Program Data> element permits the use of a suffix following the <Decimal Numeric Program Data> (NRf). The suffix expression associated units and (optional) multipliers that modify how the NRf

is interpreted by the device. The presence of a <Suffix Program Data> after an NRf is always optional. No particular <Command Program Header> or <Query Program Header> is a device shall require the use of a <Suffix Program Data> element.

4-9-6-4. Non-Decimal Numeric Program Data

The <Non-Decimal Program Data> functional element is not implemented in Model 8550. Therefore it shall not be discussed in this manual.

4-9-6-5. Arbitrary Block Program Data

The <Arbitrary Block Program Data> functional element is not implemented in Model 8550. Therefore it shall not be discussed in this manual.

4-9-6-6. Expression Program Data

The <Expression Program Data> functional element is not implemented in Model 8550. Therefore it shall not be discussed in this manual.

4-10. DEVICE-DEPENDENT COMMAND PROGRAMMING

IEEE-488.2 device-dependent commands are sent to the Model 8550 to control various operating conditions such as display modify, operating mode, output and parameter interrogate. Each command is made up of a program, command or query header followed by program data, program suffix, and terminated by program message terminator. The IEEE bus treats device-dependent commands as data in, providing that ATN is high when the commands are transmitted. For example the output amplitude is programmed by sending the following <Program Message Unit>: AMP 10.5V.

A number of <Program Message Unit> elements may be grouped together in one <Program Message> provided that each <Program Message Unit> is separated by a <Program Message Unit Separator>. <Program message Unit> elements within a <Program Message> are executed **exactly** in the same order they are received from the controller. The Model 8550 ignores all non-printable ASCII characters (00 HEX through 20 HEX) except the “CR” (carriage return). A command string is terminated by a <Program Message Terminator> which tells the instrument to execute the <Program Message>.

If an illegal <Program Header> or <Program Data> is present within a <Program Message>, the instrument will:

1. Ignore the illegal part or the <Program Message> (but will execute the rest of the <Program Message>).
2. Display an appropriate front panel error message.
3. Set certain bits in its status registers.
4. Generate an SRQ if programmed to do so.

Device-dependent programming aspects are covered in paragraph 4-8-5 and 4-10.

NOTE

Before programming the instrument over the bus, It is recommended that the instrument be set to its default values by sending an SDC or DCL over the bus. See paragraph 4-8-3 for information on using the SDC command.

In order to send a device-dependent or a common command, the controller must perform the following sequence:

1. Set ATN true.
2. Address the Model 8550 to listen.
3. Set ATN false.
4. Send the command string over the data bus one byte at a time.

NOTE

REN must be true when attempting to program the Model 8550.

Device-dependent commands that affect Models 8550 and 8551 are listed in Table 4-5. Common commands and queries are listed in Table 4-6. All the commands listed in the Tables 4-5 and 4-6 are covered in detail in the following.

4-10-1. Operating Mode (F)

The operating mode command controls the mode that the model 8550 operates. Operator may select between four different operating modes: normal operating mode, linear sweep mode, logarithmic sweep mode, and phase locking generator mode. Model 8551 has different operating modes: normal operating mode, variable duty cycle pulse generator mode, fixed duty cycle pulse generator mode, and phase locking generator mode.

The model 8550 operating mode may be programmed by sending one of the following commands:

Table 4-5. Device-Dependent Command Summary

Mode	Program Header and Data	Description
OPERATING MODE		
(Model 8550)	F0	Normal
	F1	Linear Sweep
	F2	Logarithmic Sweep
	F3	PLL
OPERATING MODE		
(Model 8551)	F0	Normal
	F1	Pulse
	F2	Fixed Duty Cycle
	F3	PLL
SWEEP DIRECTION		
(MODEL 8550)	S1	Start to Stop (up)
	S2	Stop to start (down)
	S3	Start to stop to start (up-down)
	S4	Stop to start to stop (down-up)
TRIGGER MODES		
	M1	Normal continuous mode
	M2	External Trigger
	M3	External Gate
	M4	External Burst
	M5	Internal Trigger
	M6	Internal Burst
CONTROL MODES		
	CT0	Off
	CT1	FM (Model 8550)
	CT2	AM
	CT3	PWM (Model 8551)
	CT4	VCO
OUTPUT WAVEFORMS		
	W0	DC (Model 8550)
	W1	Sinewave
	W2	Triangle
	W3	Squarewave
	W4	Fixed base-line positive squarewave
	W5	Fixed base-line negative squarewave
	W6	Ramp (Model 8551)
OUTPUT MODE		
	D0	Normal output
	D1	Disabled output
(Model 8551)	C0	Pulse/Ramp complement OFF
(Model 8551)	C1	Pulse/Ramp complement ON
EDGE CONTROL		
(Model 8551)	L0	Fastest edge transition
	L1	Linear edge transition

Table 4-5. Device-Dependent Command Summary (continued)

Mode	Program Header and Data	Description	Suffix* Data
PROGRAM PARAMETERS			
	FRQ	Program output frequency	MHZ, HZ, KHZ, MAHZ
	AMP	Program output amplitude	MV, V
	OFS	Program output offset	MV, V
	PLL	Program phase lock offset	DEG
(Model 8551 only)	PER	Program pulse period	NS, US, MS, S
(Model 8551 only)	WID	Program pulse width	NS, US, MS, S
(Model 8551 only)	DTY	Program fixed duty cycle	PCT
(Model 8551 only)	LEE	Program leading edge transition time	NS, US, MS, S
(Model 8551 only)	TRE	Program trailing edge transition time	NS, US, MS, S
	RPT	Program internal trig. generator per.	NS, US, MS, S
	BUR	Program counted burst	
	TLV	Program trigger level	V
	TPH	Program trigger phase offset	DEG
(Model 8550 only)	DCO	Program dc output level	MV, V
(Model 8550 only)	STP	Program logarithmic sweep stop	MHZ, HZ, KHZ, MAHZ
(Model 8550 only)	SWT	Program sweep time	NS, US, MS, S
(Model 8550 only)	MRK	Program logarithmic sweep marker	MHZ, HZ, KHZ, MAHZ
(Model 8550 only)	SSN	Program linear sweep stop	MHZ, HZ, KHZ, MAHZ
(Model 8550 only)	MKN	Program linear sweep marker	MHZ, HZ, KHZ, MAHZ
REVIEW PARAMETER			
	VFRQ	Display output frequency	
	VAMP	Display output amplitude	
	VOFS	Display output offset	
	VPLL	Display phase lock offset	
(Model 8551 only)	VPER	Display pulse period	
(Model 8551 only)	VWID	Display pulse width	
(Model 8551 only)	VDTY	Display fixed duty cycle	
(Model 8551 only)	VLEE	Display leading edge transition time	
(Model 8551 only)	VTRE	Display trailing edge transition time	
	VRPT	Display internal trigger generator period	
	VBUR	Display counted burst	
	VTLV	Display trigger level	
	VTPH	Display trigger phase offset	
(Model 8550 only)	VDCO	Display dc output level	
Model 8550 only)	VSTP	Display logarithmic sweep stop	
(Model 8550 only)	VSWT	Display sweep time	
(Model 8550 only)	VMRK	Display logarithmic sweep marker	
(Model 8550 only)	VSSN	Display linear sweep stop	
(Model 8550 only)	VMKN	Display linear sweep marker	

* Suffix Data is optional.

Table 4-5. Device-Dependent Command Summary (continued)

Mode	Program Header and Data	Description
RESPONSE DATA QUERY		
	FRQ?	Interrogate output frequency
	AMP?	Interrogate output amplitude
	OFS?	Interrogate output offset
	PLL?	Interrogate phase lock offset
(Model 8551)	PER?	Interrogate pulse period
(Model 8551)	WID?	Interrogate pulse width
(Model 8551)	DTY?	Interrogate fixed duty cycle
(Model 8551)	LEE?	Interrogate leading edge transition time
(Model 8551)	TRE?	Interrogate trailing edge transition time
	RPT?	Interrogate internal trig. generator period
	BUR?	Interrogate counted burst
	TLV?	Interrogate trigger level
	TPH?	Interrogate trigger phase offset
(Model 8550)	DCO?	Interrogate dc output level
(Model 8550)	STP?	Interrogate logarithmic sweep stop
(Model 8550)	SWT?	Interrogate sweep time
(Model 8550)	MRK?	Interrogate logarithmic sweep marker
(Model 8550)	SSN?	Interrogate linear sweep stop
(Model 8550)	MKN?	Interrogate linear sweep marker
(Model 8550)	ERR?	Interrogate pulse/ramp error status
	STT?	Interrogate machine status
	FSA?	Interrogate cal. failure status byte A
	FSB?	Interrogate cal. failure status byte B
	FSC?	Interrogate cal. failure status byte C
RESPONSE MESSAGE FORMAT		
	X0	Response header OFF
	X1	Response header ON
	Z0	New line (LF), END (EOI) terminator
	Z1	New line (LF) terminator
	Z2	END (EOI) terminator
	Z3	No terminator
COMMON COMMANDS		
	*CLS	Clear status command
	*ESE	Standard event status enable command
	*OPC	Operation complete command
	*RCL	Recall front panel set-up command
	*RST	Reset command
	*SAV	Save front panel set-up command
	*SRE	Service request enable command
	*TRG	Trigger command
	*WAI	Wait-to-continue command

Table 4-5. Device-Dependent Command Summary (continued)

Mode	Program Header and Data	Description
COMMON QUERIES		
	*CAL?	Calibration query
	*ESE?	Standard event status enable query
	*ESR?	Standard event status register query
	*IDN?	Identification query
	*OPC?	Operation complete query
	*SRE?	Service request enable query
	*STB?	Read status byte query
	*TST?	Self-test query
STANDARD EVENT STATUS ENABLE REGISTER MASK		
	*ESE0	No mask
	*ESE1	ESB bit set on operation complete
	*ESE2	Not used
	*ESE4	ESB bit set on query error
	*ESE8	ESB bit set on device dependent error
	*ESE16	ESB bit set on execution error
	*ESE32	ESB bit set on command error
	*ESE64	ESB bit set on user request
	*ESE128	ESB bit set on power on
CALIBRATION FAILURE STATUS BYTE A MASK		
	FSA0 through FSA16383	Mask not available
CALIBRATION FAILURE STATUS BYTE B and C MASK		
	FSB0 through FSB255	Mask not available
	FSC0 through FSC16383	Mask not available
SERVICE REQUEST ENABLE REGISTER MASK		
	*SRE0	No mask
(Model 8551 only)	*SRE1	RQS/MSS bit set on ERR bit
	*SRE2	RQS/MSS bit set on FSC bit (fail status byte C)
	*SRE4	RQS/MSS bit set on FSB bit (fail status byte B)
	*SRE8	RQS/MSS bit set on FSA bit (fail status byte A)
	*SRE16	RQS/MSS bit set on MAV bit (message available)
	*SRE32	RQS/MSS bit set on ESB bit (standard event status register)
	*SRE128	Not used

F0 = Normal operating mode
F1 = Linear sweep mode
F2 = Logarithmic sweep mode
F3 = Phase locking generator mode

The model 8551 operating mode may be programmed by sending one of the following commands:

F0 = Normal operating mode
F1 = Variable duty cycle pulse generator mode
F2 = Fixed duty cycle pulse generator mode
F3 = Phase locking generator mode

4-10-2. Sweep Direction (S)

Model 8550 while being used in one of its sweep modes provides a selection from four different sweep directions. The sweep direction command controls the direction of which the output will sweep. The sweep direction may be programmed by sending one of the following commands:

S0 = Sweep from start frequency to stop Frequency - up
S1 = Sweep from stop frequency to start Frequency - down
S2 = Sweep from start frequency to stop Frequency to start frequency - up-down
S3 = Sweep from stop frequency to start Frequency to stop frequency - down-up

4-10-3. Trigger Modes (M)

The trigger mode command gives the user control over the output stimulant of the Model 8550. There are a number of acceptable external sources for stimulating the output of the function generator. The instrument may also be set to operate in continuous mode or with having an internal trigger source. The generator may be programmed to accept either an external stimulant or an internal stimulant. Program the Model 8550 to one of the trigger modes by sending one of the following commands:

M1 = Normal continuous mode
M2 = External trigger
M3 = External gate
M4 = External burst
M5 = Internal trigger
M6 = Internal burst

4-10-4. Control Modes (CT)

Model 8550 provides three control modes: FM, AM, and VCO. Model 8551 offers PWM, Am, and VCO. The control mode command gives the user control over the control mode of the function generator. Program the Model 8550 to one of the control modes by sending one of the following commands:

CT0 = Normal operating mode
CT1 = FM mode (model 8550 only)
CT2 = AM mode
CT3 = PWM mode (model 8551 only)
CT4 = VCO mode

4-10-5. Output Waveforms (W)

The output waveform command give the user control over the output waveform. The seven parameters which are associated with the waveform commands, set the instrument to output sinewave, triangle, squarewave, positive pulse, negative pulse, DC (model 8550 only), and ramp (model 8551 only). The output waveform may be programmed by sending one of the following commands:

W0 = DC output (model 8550 only)
W1 = Sinewave
W2 = Triangle
W3 = Square wave
W4 = Fixed base-line positive square wave
W5 = Fixed base-line negative square wave
W5 = Ramp output (model 8551 only)

4-10-6. Output Mode (D, C)

The output mode command places the function generator in stand by mode. In model 8551 this command places the output in pulse complement mode and in inverted ramp mode. The output mode may be programmed by sending one of the following commands

D0 = Normal output
D1 = Disabled output
C0 = Pulse/Ramp complement OFF (mode 8551 only)
C1 = Pulse/Ramp Complement ON (model 8551 only)

4-10-7. Edge Control (L)

Model 8551, when set to operate as a pulse generator, may be placed in linear transition times mode. Rise or fall times may be independently controlled for each edge or be set to fixed (fast) transitions. The edge control command places the pulse generator in linear transition times mode. Model 8551 may be programmed by sending one of the following commands

L0 = Fastest edge transitions
L1 = Linear edge transitions

4-10-8. Parameter Programming

The parameter programming command sets the function generator to the various levels which are required for the unit under test. There are 19 different parameters which may be modified using this command. The command message unit is comprised of three parts: the <command program header>, the <decimal numeric program data>, the <suffix program data> (optional), and the <program message terminator>.

The <command program header> mnemonic is independent of control location on the front panel but relates to front panel nomenclature. For example, FRQ mnemonic is related to front panel Frequency marking.

The <decimal numeric program data> is a flexible version of numeric representation denoted by NRf. Operator may choose to program <decimal numeric program data> using NR1, NR2, or NR3 formats. Examples of the various <decimal numeric program data> is given in the following.

NR1 elements consists of a set of implicit point representations of numeric values. i.e. (±)12345.

NR2 elements are the representations of explicit point numeric values. i.e. (±)12.345.

NR3 elements are representations of scaled explicit radix point numeric values together with an exponent notation. i.e. (±)123.456E(+/-)3.

The <suffix program data> element permits the use of suffix following the NRf. The suffix expresses associated units and (optional) multipliers that modify how the NRf is interpreted by the device.

For an example, to program the model 8550 for a frequency output of 10.7 MHz, the following <program message unit> options may be used:

FRQ 10.700000; or
FRQ 10.7MAHZ; or
FRQ 10.7E+6; or
FRQ 10.7E6HZ; etc.

<Command program header> and <suffix program data> and (optional) multipliers summary is given in the following

FRQ ...MHZ, HZ, KHZ, MAHZ = Program frequency parameter
AMP ...MV, V = Program amplitude parameter
OFS ...MV, V = Program offset parameter
PLL ...DEG = Program phase lock offset parameter
PER ...NS, US, MS, S = Program pulse period parameter (model 8551 only)
WID ...NS, US, MS, S = Program pulse width parameter (model 8551 only)
DTY ...PCT = Program fixed duty cycle parameter (model 8551 only)
LEE ...NS, US, MS, S = Program leading edge transition time parameter (model 8551 only)
TRE ...NS, US, MS, S = Program trailing edge transition time parameter (model 8551 only)
RPT ...NS, US, MS, S = Program internal trigger generator period parameter
BUR ... = Program counted burst parameter
TLV ...MV, V = Program trigger level parameter
TPH ...DEG = Program trigger phase offset parameter
DCO ...MV, V = Program dc output level parameter (model 8550 only)
STP ...MHZ, HZ, KHZ, MAHZ = Program logarithmic sweep stop parameter (model 8550 only)
SWT ...NS, US, MS, S = Program sweep time parameter (model 8550 only)
MRK ...MHZ, HZ, KHZ, MAHZ = Program logarithmic sweep marker parameter (model 8550 only)
SSN ...MHZ, HZ, KHZ, MAHZ = Program linear sweep stop parameter (model 8550 only)
MKN ...MHZ, HZ, KHZ, MAHZ = Program linear sweep marker parameter (model 8550 only)

The programming limits for each of the above parameters are listed in Table 3-2. After DCL or SDC, the instrument defaults to its factory selected values. Factory defaults are listed in Table 3-1 and 4-4.

4-10-9. Display Parameter (V)

The display parameter command controls what the Model 8550 places on the display. The display parameter mode may be programmed by sending one of the following commands. The numbers in parenthesis represent the value of V in the Machine Status String - STT.

VFRQ = Display output frequency parameter (01)
VAMP = Display output amplitude parameter (02)
VOFS = Display output offset parameter (03)
VPLL = Display phase lock offset parameter (04)
VPER = Display pulse period parameter - model 8551 only (05)
VWID = Display pulse width parameter - model 8551 only (06)
VDTY = Display fixed duty cycle parameter - model 8551 only (07)
VLEE = Display leading edge transition time parameter - model 8551 only (08)

VTRE = Display trailing edge transition time parameter - model 8551 only (09)
VRPT = Display internal trigger generator period parameter
VBUR = Display counted burst parameter
VTLV = Display trigger level parameter
VTPH = Display trigger phase offset parameter
VDCO = Display dc output level parameter (model 8550 only)
VSTP = Display logarithmic sweep stop parameter (model 8550 only)
VSWT = Display sweep time parameter (model 8550 only)
VMRK = Display logarithmic sweep marker parameter (model 8550 only)
VSSN = Display linear sweep stop parameter (model 8550 only)
VMKN = Display linear sweep marker parameter (model 8550 only)

4-10-10. Common Commands

As discussed in previous paragraphs most instruments and devices in an ATE system use similar commands which perform identical functions to avoids the problem in which devices from various manufacturers used a different set of commands to enable functions and report status. Some common commands and queries, however, are optional; most of them are mandatory. Common commands and queries are listed in Table 4-6. The following set of common commands are utilized in the model 8550 (optional common commands that are not included in the model 8550 command set will not be discussed here).

***CLS** (Clear Status Command) - clears status data structures, and forces the device to the Operation Complete Command/Query Idle State. If the Clear Status command immediately follows a <Program Message Terminator>, the Output Queue and the MAV bit will be cleared.

***ESE** (Standard Event Status Enable Command) - followed by a number in the range of 0 to 255, sets the Standard Event Status Enable Register bits. The binary equivalent of the number represents the values of the individual bits set into the Standard Event Status Enable register.

***OPC** (Operation complete Command) - causes the device to generate the operation complete message in the Standard Event Status Register when all pending selected device operations have been finished.

***RCL** (Recall Command) - restores the state of the device to a state previously stored in the device's memory. If the device has more than one memory register, the command must be followed by a number to specify which register is to be used. The functions

Table 4-6. Common Commands and Queries Summary

Mode	Program Header and Data	Suffix* Data	Description
COMMON COMMANDS	*CLS		Clear status command
	*ESEn		Standard event status enable command
	*OPC		Operation complete command
	*RCLn		Recall front panel set-up command
	*RST		Reset command
	*SAVn		Save front panel set-up command
	*SREn		Service request enable command
	*TRG		Trigger command
	*WAI		Wait-to-continue command
COMMON QUERIES	*CAL?		Calibration query
	*ESE?		Standard event status enable query
	*ESR?		Standard event status register query
	*IDN?		Identification query
	*OPC?		Operation complete query
	*SRE?		Service request enable query
	*STB?		Read status byte query
	*TST?		Self-test query

restored by the *RCL command are the same as those affected by the *RST command. Model 8550 may recall settings in registers designated with numbers from 00 to 30.

***RST** (Reset) - Sets device-dependent functions to a known state, purges all *OPC commands and queries, and aborts all pending operations. The output queue, Service Request Enable Register, Standard Event Status Enable Register, and power-on flag are not affected. Device defaults are listed in Table 4-4

***SAV** (Save Command) - allows the user to store the present state of a device in local memory. If the device has more than memory location, the command must be followed by a number to designate the storage register to be used. Model 8550 may store settings in registers designated with numbers from 00 to 30.

***SRE** (Service Request Enable Command) - followed by a number, sets the Service Request Enable register which determines what bit in the status byte will cause a service request from the device. The binary equivalent of the number represents the values of the individual bits of the Service Request Enable Register.

***TRG** (Trigger Command) - has exactly the same effect as a GET when received, parsed, and executed by the device.

***WAI** (Wait to Continue Command) - causes a device to wait until all previous commands and queries are completed before executing any which follow the *WAI command.

4-10-10-1. Set-ups (*SAV, *RCL)

The setups commands select the memory location where front panel setup is to be stored (*SAV) or from where recalled (*RCL). To store or recall a setup use one of the following commands:

***SAVnn**
***RCLnn**

Where nn may range from 00 to 30. nn is the selected memory cell of which the setup is to be stored or from where the setup is to be recalled.

4-11. DEVICE TALKING FORMATS

This paragraph discusses the formatting of <Response Message> elements sent from a device via its system interface. Allowable IEEE-488.2 response message is composed of a sequence of <Response Message> units, each unit representing a response to a query. Each <Response Message> is composed of a sequence of functional syntactic elements. Legal IEEE-488.2 <Response Message> is created from functional elements sequences. A <Response Message is interpreted by a controller running an application program, and as such, needs to convey its information precisely for consistent operation with a wide range of controllers. A <Response Message>, therefore, has a more restrictive format than a <Program Message>.

Some queries of universal instrument system application have been defined by the IEEE-488.2. They are the common queries; these queries are specific path selections through the functional syntax diagram as specified in the IEEE-488.2 standard. The remaining queries are device-specific and are generated by the device designer using the functional syntax diagram and the needs of the device. The functional elements include separators, terminators, headers, and data types. These elements are discussed in the following.

4-11-1. Functional Element Summary

<Response Message> Represents a sequence of one or more <Response Message Unit> elements separated by <Response Message Unit Terminator> elements.

<Response Message Unit> Represents a single message unit sent from the device.

<Response Data> Represents any of the eleven different <Response Data> types.

<Response Message Unit Separator> Separates <Response Message Unit> elements from one another in a <Response Message>.

<Response Data Separator> Separates sequential <Response Data> elements that are related to the same header or to each other.

<Response Header Separator> Separates the header from the associated <Response Data>.

<Response Message Terminator> Terminates a <Response Message>.

<Response Header> Specifies the function of the associated <Response Data> element(s). Alpha characters mnemonically indicate the function.

<Character Response Data> A data type suitable for sending short mnemonic character strings. Generally used when a numeric data type is not suitable.

<Decimal Numeric Response Data> A data type response suitable for sending decimal integers or decimal fractions with or without exponents.

<NonDecimal Numeric Response Data> A data type suitable for sending integer numeric representation in base 16, 8, or 2. Useful for data that is more easily interpreted when directly expressed in a non-decimal format.

<String Response Data> A data type suitable for sending 7-bit ASCII character strings where the content needs to be "Hidden" (by delimiters). This element is generally used to send data for direct display on a device.

<Definite Length Arbitrary Block Response Data> A data type suitable for sending blocks of arbitrary 8-bit information when the length is known beforehand.

<Indefinite Length Arbitrary Block Response Data> A data type suitable for sending blocks of arbitrary 8-bit information when the length is not known beforehand or when computing the length beforehand is undesirable.

<Arbitrary ASCII Response data> A data type suitable for sending arbitrary ASCII data bytes when alternate data types are unworkable.

4-11-2. Separator Functional Element Summary

The various elements within the <Response Message> are separated by ASCII characters that were specially assigned for this purpose. These separators are discussed in the following paragraphs.

4-11-2-1. Response Message Unit Separator

The <Response Message Unit Separator> separates sequential <Response Message Unit> elements from one another when multiple <Response Message Unit> elements are sent in a <Response Message>. The <Response Message Unit Separator> is defined as:

;

4-11-2-2. Response Data Separator

The <Response Data Separator> separates sequential <Response Data> elements from one another when multiple data elements are sent. The <Response Data Separator> is defined as:

,

4-11-2-3. Response Header Separator

The <Response Header Separator> separates the <Response Header> from the <Response Data>. The <Response Header Separator> is defined as:

<Space>

4-11-3. Response Message Terminator

The <Response Message Terminator> element's function is to terminate a sequence of one or more <Response Message Unit> elements. There are three possible <Response Message Terminator> elements:

1. NL (new line);
2. NL END (EOI); and
3. END (EOI)

NL is defined as a single ASCII-encoded byte 0A (10 decimal). Leading <White Space> elements are not permitted. The instrument interprets any and all of the three terminators as semantically equivalent. No alternative encoding are allowed. Note that IEEE-P981 amendment forbids the use of CR as a <Response Message Terminator> element. This is because some controller treat CR as the end of transmission and leave the LF character in the unit, thereby creating an error in the controller.

4-11-4. Response Header

The <Response Header> is available for use by the device designer for device-specific responses. It may be used, for example, to create responses in directly resendable <Program Message Unit> format or to identify response data to the controller. There are three defined <Response Header> elements: <Simple Response Header>, <Compound Response Header>, and <Common Response Header. A <Simple Response Header> is defined as:

<Response Mnemonic>

For example, FRQ. Leading <White Space> elements are not permitted. Upper/lower case alpha characters are treated with the same semantic equivalence. <Compound Response Header> is not used in model 8550 and will not be discussed here. A <Common Response Header> is defined as:

***<Response Mnemonic>**

For example, *SRE. Leading <White Space> elements are not permitted. Upper/ lower case alpha characters are treated with the same semantic equivalence.

4-11-5. Response Data

A <Response Data> functional element is used to convey a variety of response information related to the <Response Header>. The element type is determined by the eliciting query. <Non-Decimal Response Data>, <String Response Data>, and <Arbitrary Block Response Data> functional elements are not implemented in Model 8550. Therefore it shall not be discussed in this manual.

4-11-5-1. Character Response Data

The <Character Response Data> functional element is used to convey information best expressed

mnemonically as a short alpha or alphanumeric string. It is useful when numeric parameters are inappropriate, for example, model number and manufacturer identification.

4-11-5-2. Decimal Numeric Response Data

The <Decimal Numeric Response Data> is a flexible version of the three numeric representations as defined in ANSI X3.42-1975 - NR1, NR2, and NR3. A <Decimal Numeric Response Data> elements are defined as:

1. NR1 elements consists of a set of implicit point representations of numeric values. i.e. (±)12345.

2. NR2 elements are the representations of explicit point numeric values. i.e. (±)12.345.

3. NR3 elements are representations of scaled explicit radix point numeric values together with an exponent notation. i.e. (±)123.456E(±)3.

4-12. READING FROM THE MODEL 8550

The reading sequence is used to obtain, from Model 8550, various <Response Message Units> such as frequency, amplitude, offset or operating modes. The <Response Message Unit> elements are placed in an output queue. The output queue may be read by device-defined queries. Such device-defined queries cause the item read to be removed from the output queue. Model 8550 executes the <Program Message> elements in the order received. The output is cleared when any of the following occur:

1. Reading all the items in the output queue.
2. Upon receipt of a new <Program Message>.
3. Upon receipt of the *CLS, DCL or SDC commands.
4. Upon Power on.

IEEE-488.2 specifies that a device cannot send <Response Message> elements unless commanded to do so. This is specified as an “Unterminated Action”. The “Unterminated Action” is executed when the controller attempts to read a <Response Message> from the device without first having sent a complete Query Message, including the <Program Message Terminator>, to the device. In the event of “Unterminated Action” model 8550 performs the following steps:

1. Sets the Query Error bit in the Standard Event Status Register.
2. Clears the output queue.
3. Sets **brq** False.

If a read sequence is interrupted by a new <Program Message> before it finishes sending a <Response Message>, model 8550 executes an “Interrupted Action”. GPIB bus response is similar to the “Unterminated Action”.

The reading sequence is conducted as follows:

1. The controller sets the ATN line true.
2. The Model 8550 is addressed to talk.
3. The controller sets ATN false.
4. The instrument sends the information string over the bus one byte at a time.
5. The controller recognizes that the string is terminated.
6. The controller sets the ATN line true.
7. The UNT (untalk) command is placed on the bus by the controller.

4-12-1. Interrogate Parameter Data Query

The interrogate parameter data query allows access to information concerning present operating conditions of the instrument. When the interrogate parameter data query is given, the Model 8550 will transmit appropriate data string information the next time the instrument is addressed to talk. Model 8550 Interrogate Parameter Data Query include:

FRQ?	=	Interrogate output frequency parameter
AMP?	=	Interrogate output amplitude parameter
OFS?	=	Interrogate output offset parameter
PLL?	=	Interrogate phase lock offset parameter
PER?		Interrogate pulse period parameter (model 8551 only)
WID?		Interrogate pulse width parameter (model 8551 only)
DTY?		Interrogate duty cycle dat string (model 8551 only)
LEE?		Interrogate leading edge transition time parameter (model 8551 only)
TRE?		Interrogate trailing edge transition time parameter (model 8551 only)
RPT?		Interrogate internal trigger generator period parameter
BUR?		Interrogate counted burst parameter
TLV?		Interrogate trigger level parameter
TPH?		Interrogate trigger phase offset parameter
DCO?	=	Interrogate dc output level parameter (model 8550 only)
STP?	=	Interrogate logarithmic sweep parameter (model 8550 only)
SWT?	=	Interrogate sweep time parameter (model 8550 only)
MRK?	=	Interrogate logarithmic sweep marker parameter (model 8550 only)
SSN?	=	Interrogate linear sweep stop parameter (model 8550 only)

MKN? Interrogate linear sweep marker parameter (model 8550 only)
EER? Interrogate pulse/ramp error (model 8551 only)
STT? Interrogate machine status
FSA? Interrogate calibration failure status byte A
FSB? Interrogate calibration failure status byte B
FSC? Interrogate calibration failure status byte C

For example, model 8550 is asked to return frequency, amplitude, and offset parameters in a single <Response Message>

Command: FRQ?;AMP?
Response:FRQ 1.000E+3;AMP 1.00E+0

Table 4-7 shows the general <Response Message> format for each of the above commands. Default values are shown. These defaults are generated after an SDC or DCL commands.

4-12-2. Common Queries

As discussed in previous paragraphs most instruments and devices in an ATE system use similar commands which perform identical functions to avoids the problem in which devices from various manufacturers used a different set of commands to enable functions and report status. Some common commands and queries, however, are optional; most of them are mandatory. The following set of common queries are utilized in the model 8550 (optional common queries that are not included in the model 8550 command set will not be discussed here).

***CAL?** (Calibration Query) - causes a device to perform an internal self-calibration and generate a response that indicated whether or not the device completed the self-calibration without error. The calibration errors are stored in an internal 8-bit register which is not accessible by device-dependent or common queries. Each bit in this register represents an error in a different block within the model 8550.

The generator responds to this query with a number in the range of 0 to 32767. The binary equivalent of the number represents the detected error in the calibration process. For example, if a value of 32 indicates a calibration failure in the pulse width circuit. Similarly, A value of 24 indicates a calibration error in the PLL and trigger circuits. A value of 0 in the response indicates that the calibration was carried out successfully. Note that complete information on calibration errors are available in the Calibration Failure Status Registers. These auxiliary status registers are discussed in-details later in this section. The calibration query does not require any local operator interaction to function. Upon completion of *CAL?, the device returns to the state just prior to the calibration cycle. The various bits in the calibration error register are listed in the following.

Table 4-7. Response Message Format Summary

Command	Response Format (*)
FRQ?	FRQ 1.000E+3(terminator)
AMP?	AMP 1.00E+0(terminator)
OFS?	OFS 0.00E+0(terminator)
PLL?	PLL 00E+0(terminator)
PER?	PER 1.000E-3(terminator)
WID?	WID 10.00E-3(terminator)
DTY?	DTY 50E+0(terminator)
LEE?	LEE 10.0E-6(terminator)
TRE?	TRE 10.0E-6(terminator)
RPT?	RPT 1.00E+0(terminator)
BUR?	BUR 2E+0(terminator)
TLV?	TLV 1.6E+0(terminator)
TPH?	TPH 00E+0(terminator)
DCO?	DCO 0.00E+0(terminator)
STP?	STP 9.000E+3(terminator)
SWT?	SWT 1.00E+0(terminator)
MRK?	MRK 5.000E+0(terminator)
SSN?	SSN 9.000E+3(terminator)
MKN?	MKN 5.000E+0(terminator)
ERR?	ERR 00000000(terminator)
FSA?	FSA 00000000(terminator)
FSB?	FSB 00000000(terminator)
FSC?	FSC 00000000(terminator)

(*) NL END is normal terminator. Terminator may change (see paragraph 4-12-4).

Bit 0 - Frequency calibration error.
Bit 1 - Amplitude calibration error.
Bit 2 - Offset calibration error.
Bit 3 - PLL calibration error.
Bit 4 - Trigger calibration error.
Bit 5 - Pulse width calibration error.
Bit 6 - Rise/Fall time calibration error.
Bit 7 - Not used

***IDN?** (Identification Query) - Causes the generator to respond with its identity. The returned data is organized into four fields, separated by commas. The unit must respond with its manufacturer and model number in the first two fields and may also report its serial number and options in field three and four. If the later information is not available, the

device must return an ASCII 0 for each. For example, model 8551 response to *IDN? is Tabor,8551,0,REV1.1.

***OPC?** (Operation Complete Query) - causes the device to generate the operation complete message in the Standard Event Status Register when all pending selected device operations have been finished.

***SRE?** (Service Request Enable Query) - enables the user to read the contents of the Service Request Enable register. The device returns a number in the range of 0 to 63 or 128 to 191, since bit 6 (RSQ) cannot be set. The binary equivalent of the number represents the value of the bits of the Service Request Enable Register.

***STB?** (Read Status Byte Query) - Reads the status byte containing the master summary status (MSS) bit. The device responds with an integer in the range of 0 to 255, whose binary equivalent represents the value of the bits of the status byte.

***TST?** (Self-Test Query) - Tells the device to perform an internal self-test and report back to the controller if any errors are detected. The generator responds to this query with a number. A value of 1 in the response indicates that the self-test routine has detected an error. A value of 0 in the response indicates that the self-test was carried out successfully.

4-12-3. Response Header (X)

The <Response Header> from the <Response Message> string may be suppressed using this command. When the <Response Header> is suppressed the output data string is 3 byte shorter. The <Response Header> may be suppressed using the following commands:

X0 = Response header OFF
X1 = Response header ON

4-12-4. Response Message Terminator (Z)

To allow a wide variety of controllers to be used, the terminator can be changed by sending the appropriate command over the bus. The default value is New Line (LF), End (EOI) sequence (mode Z0). The terminator sequence will assume this default value after receiving a DCL or SDC.

The EOI (END) line on the bus is usually set low by the device during the last byte of its data transfer sequence. In this way, the last byte is properly identified, allowing variable length data words to be transmitted. The Model 8550 will normally send EOI during the last byte of its data string or status word. The <Response Message Terminator> in model 8550 may be programmed by sending one of the following commands:

Z0 = New Line (LF), END (EOI) terminator
Z1 = New Line (LF) terminator
Z2 = END (EOI) terminator
Z3 = No terminator

NOTES

1. Most controllers use the LF character to terminate their input sequence. Using the NO TERMINATOR mode (Z3) may cause the controller to hang up unless special programming is used.
2. Some controllers may require that EOI be present at the end of the string.

4-13. DEVICE STATUS REPORTING

Device status reporting defined by IEEE-488.2 builds upon and extends the original specifications of the status byte of the IEEE-488.1 document. A complete model is defined for all status reporting. Figure 4-3 illustrates the IEEE-488.2 status reporting model showing the IEEE-488.1 status byte, which can be read by either a serial poll or Status Byte Query. Summary of related common commands and queries is given in the following.

***STB?** - Returns an NR1, which is the value of the IEEE-488.1 status byte and the MSS (Muster Summary Status) summary message.

***OPC** - Sets the Operation Complete event bit in the Standard Event Status Register when all selected pending device operation have been completed.

***OPC?** - Places a “1" in the output queue when all selected pending operations are completed which in turn cause the MAV (Message Available) summary message to be generated.

***CLS** - Clears all Event Registers summarized in the status byte.

***ESR?** - Returns an NR1, which is the value of the Standard Event Status Enable Register.

***SRE NRf** - Sets the bits of the Service Request Enable Register.

***SRE?** - Returns an NR1, which is the value of the Service Request Enable Register.

4-14. STATUS BYTE REGISTER (STB)

The Status Byte Register contains the device’s STB and RQS (or MSS) messages. IEEE-488.1 defines the method of reporting the STB and RQS, but leaves the setting and clearing protocols and semantics for the STB message undefined. The standard

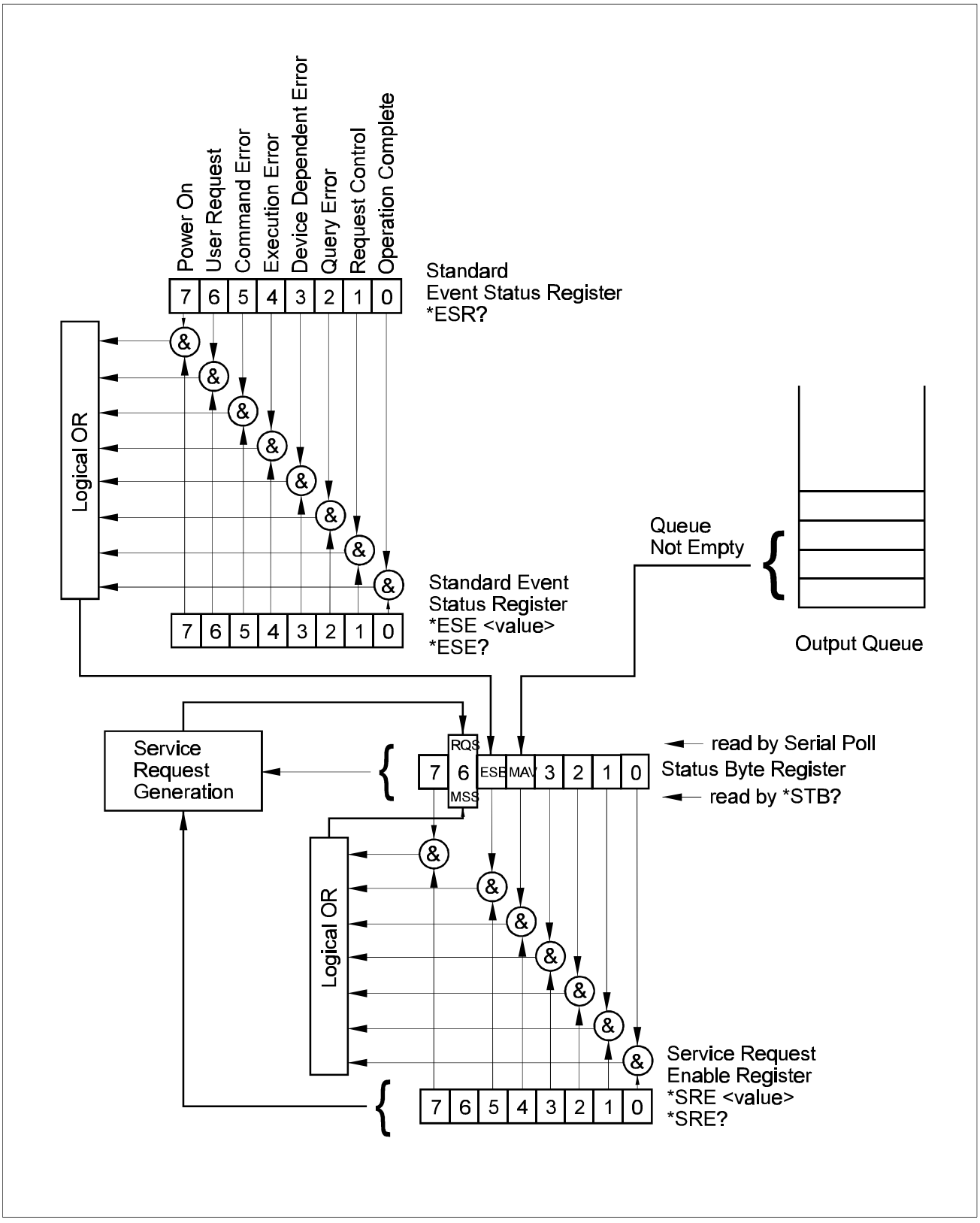


Figure 4-3. IEEE-488.2 Status Reporting Model

further defines specific device STB summary-messages.

A Muster Summary Status (MSS) message is also provided which is output as bit 6 with the STB response to a *STB? common query. The Status Byte Register is altered only when the state of the overlaying Status Data Structure is altered. The description of the various bits within the Status Byte Register is given in the following.

Bit 0 - Pulse/Ramp Error Status Summary. The state of this bit indicates whether or not a pulse/ramp programming error in the Pulse/Ramp Error Status Register (ERR) have occured. The ERR summary message is true when a pulse/ramp programming error have been detected.

Bit 1 - Calibration Failure Status Summary C. The state of this bit indicates whether or not a calibration failure in the Calibration Failure Status Byte C (FSC) have occurred. The FSC summary-message is true when a calibration error was have been detected.

Bit 2 - Calibration Failure Status Summary B. The state of this bit indicates whether or not a calibration failure in the Calibration Failure Status Byte B (FSB) have occurred. The FSB summary-message is true when a calibration error was have been detected.

Bit 3 - Calibration Failure Status Summary A. The state of this bit indicates whether or not a calibration failure in the Calibration Failure Status Byte A (FSA) have occurred. The FSA summary-message is true when a calibration error was have been detected.

Bit 4 - **Message Available Queue Summary Message (MAV)**. The state of this bit indicates whether or not the output queue is empty. The MAV summary-message is true when the output queue is not empty. This message is used to synchronize information exchange with the controller. The controller can, for example, send a query command to the device and then wait for MAV to become true. If an application program begins a read operation of the output queue without first checking for MAV, **all system bus** activity is held up until the device responds.

Bit 5 - **Standard Event Status Bit (ESB) Summary Message**. The ESB summary message is an IEEE-488.2 defined message. Its state indicates whether or not one or more of the enabled ESB events have occurred since the last reading or clearing of the Standard Event Status Register.

Bit 6 - Master Summary Status (MSS)/Request Service (RQS) Bit. Its state indicate if the device has at least one condition to request service. The MSS bit is not part of the IEEE-488.1 status byte and will not be sent in response to a serial poll. The RQS bit, however, if set, will be sent in response to a serial poll.

Bit 7 - Not used.

4-14-1. Reading the Status Byte Register

The Status Byte Register can be read with either a serial poll or the *STB? common query. Both of these methods read the IEEE-488.1 STB message. The value sent for the bit 6 position is, however, dependent upon the method used.

4-14-1-1. Reading with a Serial Poll

When serial polled, the generator returns the 7-bit status byte plus the single bit RQS message. The status bye and RQS message are returned to the controller as a single data byte. The RQS message is sent on line D107 (bit 6). **RQS TRUE** means that bit 6 line is asserted (pulled to a low voltage) when the status byte is sent. The response represents the sum of the binary-weighted values of the Status Byte Register.

Reading the Status Byte Register with a serial poll sets the RQS message FALSE until a new reason for service has occurred. The STB portion of the Status Byte Register is read non-destructively. The value of the status byte is not altered by a serial poll. Once the model 8550 has generated an RQS, its status byte should be read to clear the SRQ line so the controller can detect an SRQ from another device. Otherwise the instrument will continuously assert the SRQ line.

4-14-1-2. Reading with the *STB?

The *STB? common query causes the generator to send the contents of the Status Byte Register and the MSS (Master Summary Status) summary message as a single <NR1 Numeric Response Message> element. The response represents the sum of the binary-weighted values of the Status Byte Register. The *STB? common query does not alter the status byte.

4-14-1-3. Clearing the Status Byte Register

The entire Status Byte Register can be cleared by removing the reasons for service from the Auxiliary Status Registers. Sending the *CLS common command to the device after a <Program Message Terminator> and before <Query Message Unit> ele-

ments clears the Standard Event Status Register and clears the output queue of any unread messages. With the output queue empty, the MAV summary message is set to FALSE.

Methods of clearing the other auxiliary status registers are discussed in the following. The RQS message in the Status Byte Register will be FALSE. The use of the IEEE-488.1 DCL or SDC commands another method of clearing the Status Byte Register, however, in some cases it is not recommended to use this method since the entire front panel set-up is reset to factory default values.

4-14-1-4. Service Request Enable Register

The Service Request Enabling Register is an 8-bit register that enables corresponding summary messages in the Status Byte Register. Thus, the application programmer can select reasons for the model 8550 to issue a service request by altering the contents of the Service Request Enable Register.

The Service Request Enable Register is read with the ***SRE?** common query. The response to this query is an number that represents the sum of the binary-weighted value of the Service Request Enable Register. The value of the unused bit 6 is always zero.

The Service Request Enable Register is written using the ***SRE** common command followed by a <Decimal Numeric Program Data> element representing the bit values of the Register. A bit value one indicates an enabled condition. Consequently, a bit value of zero indicates a disabled condition. The Service Request Enable Register is cleared by sending *SRE0. The generator always ignores the value of bit 6. Summary of *SRE messages is given in the following.

***SRE0** - No mask.
***SRE1** - Service request on pulse/ramp error.
***SRE2** - Service request on FSC.
***SRE4** - Service request on FSB.
***SRE6** - Service request on FSA.
***SRE16** - Service request on MAV.
***SRE32** - Service request on ESB.
***SRE128** - Not used.

4-14-2. Standard Event Status Register (ESR)

The Standard Event Status Register is a special application of the status reporting. IEEE-488.2 document specifies the meaning of each bit of this register. The 8 bits of the SESR have been defined by the IEEE-488.2 as specific conditions which can be monitored and reported back to the user upon request.

The Standard Event Status Register is destructively read with the ***ESR?** common query. The Standard Event Status Register is cleared by a ***CLS** common command, on power-on, and when read by *ESR?.

The arrangement of the various bits within the register is firm and is required by all GPIB instruments that implement the IEEE-488.2. Description of the various bits is given in the following.

Bit 0 - Operation Complete. Generated in response to the *OPC command. It indicates that the device has completed all selected and pending operations and is ready for a new command.

Bit 1 - Request Control. This bit operation is disabled on model 8550.

Bit 2 - Query Error. This bit indicates that an attempt is being made to read data from the output queue when no output is either present or pending.

Bit 3 - Device Dependent Error. This bit is set when an error in a device function occurs. For example, the following <Program Message> will cause DDE error: AMP10E+0;OFS10E+0. Both parameters are legal and within the specified limits, however, the function generator is unable to generate such an amplitude and offset combination. Following the Device Dependent Error the generator continues to process the input stream.

Bit 4 - Execution Error. This bit is generated if the <Program Data> element following the header is outside of the legal input range of the generator.

Bit 5 - Command Error. This bit indicates the generator received a command that was a syntax error, or a command that the device does not implement. A GET receive inside a <Program Message> will also cause a Command Error.

Bit 6 - User Request. This event bit indicates that one of a set of local controls, the MANUAL push-button in this case, has been activated. This event bit occurs regardless of the remote or local state of the device.

Bit 7 - Power On. This bit indicates that the device's power source was turned off, then on, since the last time that the register was read.

4-14-2-1. Standard Event Status Enable Register (ESE)

The Standard Event Status Enable Register allows one or more events in the Standard Event Status

Register to be reflected in the ESB summary-message bit. The Standard Event Status Enable Register is an 8-bit register that enables corresponding summary messages in the Standard Event Status Register. Thus, the application programmer can select reasons for the model 8550 to issue a ESB summary-message bit by altering the contents of the ESE Register.

The Standard Event Status Enable Register is read with the ***ESE?** common query. The response to this query is an number that represents the sum of the binary-weighted value of the Standard Event Status Enable Register.

The Standard Event Status Enable Register is written using the ***ESE** common command followed by a <Decimal Numeric Program Data> element representing the bit values of the Register. A bit value one indicates an enabled condition. Consequently, a bit value of zero indicates a disabled condition. The Standard Event Status Enable Register is cleared by sending *ESE0. Summary of *ESE messages is given in the following.

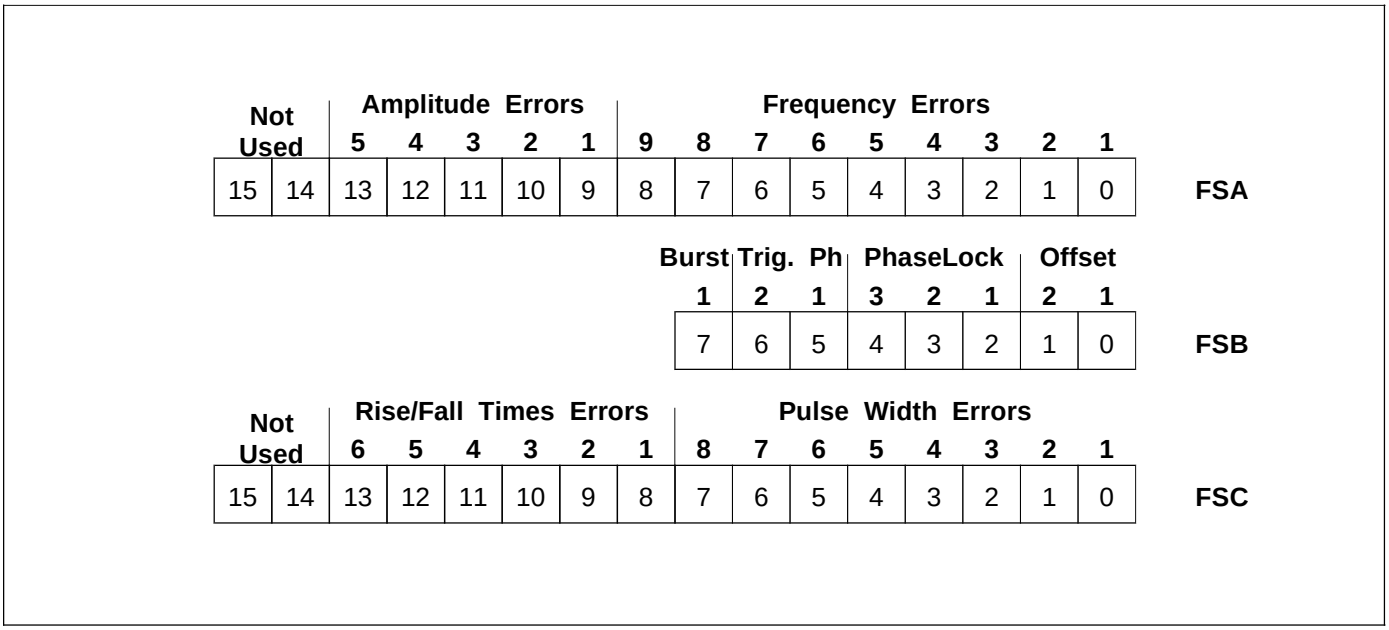
***ESE0** - No mask.
***ESE1** - ESB on Operation Complete.
***ESE2** - ESB on Request Control.
***ESE4** - ESB on Query Error.
***ESE6** - ESB on Device Dependent Error.
***ESE16** - ESB on Execution Error.
***ESE32** - ESB on Command Error.
***ESE64** - ESB on User Request.
***ESE128** - ESB Power on.

4-14-3. Calibration Failure Status Registers A (FSA), B (FSB), and C (FSC)

The Calibration Failure Status Registers FSA, FSB, an FSC are a special application of the status reporting. Figure 4-4 illustrates the calibration failure status registers. The 16 bits of the FSA contain information about calibration failures in the frequency and the amplitude circuits. The 8 bits of the FSB contain information about calibration failures in the offset, phase lock loop, trigger phase offset, and burst circuits. The 16 bits of the FSC contain information about calibration failures in the pulse width generator and the rise/fall time control circuits.

The summary-messages from these registers are fed to the Status Byte register and can be monitored and reported back to the user upon request. The Calibration Failure Status Registers are destructively read with the **FSA, FSB,** and **FSC** queries. The response to this query is a number that represents the sum of the binary-weighted value of the Calibration Failure Status Register. The Calibration Failure Status Registers are cleared by a ***CLS** common command, and when read by FSA, FSB, and FSC. Power off does not clear these registers. Description of the various calibration failures is given in the troubleshooting section of this manual.

Figure 4-4. Calibration failure Status Registers Interpretation.



There are no enable registers for the Calibration Failure Registers which are available for the programmer. Thus, whenever a calibration error occurs, the information is immediately fed to the Status Byte Register.

4-14-4. Pulse/Ramp Error Status Register (ERR)

The Pulse/Ramp Error Status Register (ERR) is a special application of the status reporting. It is available only on model 8551. Figure 4-5 illustrates the pulse/ramp errors status register. The 8 bits of the ERR contain information about programming errors of inter-related pulse or ramp <Program Data> parameters such as pulse width and period. Description of the various pulse/ramp errors is given in the following.

The ERR summary-message is fed to the Status Byte Register and can be monitored and reported back to the application programmer upon request. The ERR is **non-destructively** read with the **ERR?** query.

The response to this query is a number that represents the sum of the binary-weighted value of the Pulse/Ramp Error Status Register. The ERR register is cleared only by removing the related error that cause one or more bits in this register to be set TRUE. Power off does not clear the ERR register.

There is no enable register for the Pulse/Ramp Error Status Register which is available for the programmer. Thus, whenever such an error occurs, the information is immediately fed to the Status Byte Register.

Description of the various bits in the Pulse/Ramp Error Status Register is given int the following. When the pulse generator is set to operate in its triggered mode of operation, the period time, in the following formulas is replaced by the period of the internal trigger generator.

Error 1 (Bit 0) - This bit indicates that an error relating to the pulse width and the period have occurred. This error bit is set true under the following conditions:

Pulse Width > 0.8 x Period

Error 2 (Bit 1) - This bit indicates that an error relating to the pulse width and the period have occurred. This error bit is set true under the following conditions:

Period - Pulse Width < 10 ns

Error 3 (Bit 2) - This bit indicates that an error relating to the pulse width and the leading edge transition time have occurred. This error bit is set true under the following conditions:

1.25 x Rise Time > Pulse Width

Error 4 (Bit 3) - This bit indicates that an error relating to the pulse width, the period, and the trailing edge transition time have occurred. This error bit is set true under the following conditions:

1.25 x Fall Time > Period - Pulse Width

NOTE

When the model 8551 is placed is External Trigger mode, errors 1, 2, and 4 can not occur.

Error 5 (Bit 4) - This bit indicates that an error relating to the period (Per) counted burst (N), the trailing edge transition time (Trail), and the internal trigger period (I. Per) have occurred. This error bit is set true under the following conditions:

N x Per + Trail > I. Per

Note that in the above formula, the value of N in triggered mode is set to 1; and the value of Trail in fast transition times is set to 0.

Error 6 (Bit 5) - This bit indicates that an error relating to the ramp duration have occurred. This error bit is set true under the following conditions:

Ramp Duration > 5 μs

Error 7 (Bit 6) - This bit indicates that an error relating to the pulse width have occurred. This error bit is set true under the following conditions:

Pulse Width < 10 ns

Error 8 (Bit 7) - This bit indicates that an error relating to the pulse width have occurred. This error bit is set true under the following conditions:

Pulse Width > 999 ms

Figure 4-5. Ramp/Pulse Errors Status String (ERR) Interpretation .

Pulse/Ramp Errors

Error No.	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
Bit No.	7	6	5	4	3	2	1	0

4-14-5. Machine Status Register (STT)

The Machine Status Register (STT) is a special register which contain the present front panel setting. The STT is **non-destructively** read with the **STT?** query. The response to this query is a NR1 <Numeric Response Data> with the length of 11 digits. These digits are numeric representation of the various Machine Status options as illustrated in Figure 4-6.

4-15. FRONT PANEL ERROR MESSAGES

The process of programming the Model 8550 involves the proper use of syntax. Syntax is defined as the orderly or systematic arrangement of programming commands or languages. The Model 8550 must receive valid commands with proper syntax or it will:

1. Ignore the part of the <Program Message Unit> in which the invalid command appears.
2. Set appropriate bits in the Standard Event Status Register.
3. Generate an SRQ if programmed to do so.
4. Display an appropriate front panel message.

4-15-1. ILI (Illegal Instruction) Error

An ILI error results when the Model 8550 receives an invalid <Program Header> such as AMPL1.00. This command is invalid because the real command should read AMP1.00. When such an illegal <Program Header> is detected by the instrument, the following message will be displayed on the Model 8550 for about one second:

ILI

4-15-2. ILP (Illegal Parameter) Error

An ILP error occurs when the <Numeric Data> parameter associated with a legal <Program Header> command is not valid. For example, the command AMP100E+0 is not a valid option because the required amplitude is outside the legal limits of the model 8550. When such an illegal <Numeric Data> is detected, the following message will be displayed on the Model 8550 for about one second:

ILP

4-16. GPIB COMPATIBILITY WITH HP MODEL 8116A

Model 8551 can be made fully compatible with HP model 8116A device-dependent command set. This built-in option saves a lot of valuable programming time, when replacing model 8116A with model 8551. In other words, one can remove HP's model 8116A from an ATE-system rack and replace it with the Tabor 8550/8551, without the need to modify the existing test software. A list of device dependent command which is being used by the HP mode 8116A is given in the following. Listed are those commands that have equivalent functions in the Model 8550. For complete description of the various commands refer to Table 3-3 - Mode/Parameter Messages (listen function) - in the HP manual. To modify 8551 device-dependent command set to comply with model 8116A proceed with the following steps:

1. Depress the [2nd] push-button once then depress the [GPIB ADR] push-button. The display will be modified to display the following:

GPxx

Where x may be any number from 0 to 30.

2. Depress MODIFIER [x100 ⇑] push-button once. The displayed reading will change as follows:

HPxx

Indicating that model 8551's device-dependent command set is made fully compatible with HP's model 8116A device-dependent command set. Depressing the MODIFIER [x100 ⇑] or [x100 ⇓] push-buttons toggles between GPIB and HPIB compatibility options. To modify the GPIB address proceed with the procedure given in paragraph 4-7.

3. To store the required compatibility option depress [EXE]. The instrument then resumes normal operation.

Figure 4-6. Machine Status String (STT) Interpretation *

<Program Header>	**V**	**M**	**CT**	**W**	**L/S**	**F**	**C**	**D**	**X**	**Z**
<Progran Data>	01	1	0	1	0/1	0	0	0	0	0

* Status given after IEEE-488.1 DCL or SDC commands, or afetr IEEE-488.2 *RST common command.

Table 4-8. HP's Model 8116A - Mode/Parameter Messages

MESSAGE	MNEMONICS ASCII CODE	ASCII CODE DELIMITER	Description
Operating Modes			
	M1		Select normal
	M2		Select Trigger
	M3		Select gate
	M4		Not used in Model 8550/8551
	M5		Select internal sweep (Opt. 001)
	M6		Select external sweep (Opt. 001)
	M7		Select internal burst (Opt. 001)
	M8		Select external burst (Opt. 001)
Control Mode			
	CT0		Off
	CT1		Select FM (Model 8550 only)
	CT2		Select AM
	CT3		Select PWM (Model 8551 only)
	CT4		Select VCO
Haversine (–90°)			
	H0		Off
	H1		On
Trigger Slope			
	T0		Off (Not used in Model 8550/8)
	T1		Positive slope (Not used in Model 8550/8)
	T2		Negative slope (Not used in Model 8550/8)
Waveforms			
	W0		Off (dc) (Model 8550 only)
	W1		Select sine
	W2		Select triangle
	W3		Select Square
	W4		Select pulse
	W5		Select positive pulse
	W6		Select negative pulse
Parameters(*)			
	FRQ	MZ = Millihertz HZ = Hertz KHZ = Kilohertz MHZ = Megahertz	Set frequency
	DTY	%	Set duty cycle (Model 8551 only)
	WID	NS = Nanoseconds US = Microseconds MS = Milliseconds	Set width (Model 8551 only)
	AMP	MV = Millivolts V = Volts	Set amplitude
	OFS	MV = Millivolts V = Volts	Set offset
	HIL	V = Volts	Set high level

Table 4-8. HP's Model 8116A - Mode/Parameter Messages (continued)

MESSAGE	MNEMONICS ASCII CODE	ASCII CODE DELIMITER	Description
Parameters(*) (Opt. 001)	BUR	#	Set burst number
	RPT	NS = Nonoseconds US = Microseconds MS = Milliseconds	Set repetition rate for internal burst
	STA	MZ = Millihertz HZ = Hertz KHZ = Kilohertz MHZ = Megahertz	Set sweep start frequency (Model 8550)
	STP	MZ = Millihertz HZ = Hertz KHZ = Kilohertz MHZ = Megahertz	Set sweep stop frequency (Model 8550)
	MRK	MZ = Millihertz HZ = Hertz KHZ = Kilohertz MHZ = Megahertz	Set sweep marker frequency (Model 8550)
	SWT	S = Seconds MS = Milliseconds	Set sweep time (Model 8550)
Limit	L0		Off
	L1		On
Complement	C0		Off (normal output, Model 8551 only))
	C1		On
Disable	D0		Off (output enable)
	D1		On
Autovernier Mode	A0		Off
	A1		On
Autovernier Start	MU		Most significant digit up
	SU		Second significant digit up
	LU		Least significant digit up
	MD		Most significant digit down
	SD		Second significant digit down
	LD		Least significant digit down
Execute Self Test	EST		
Current Parameter Setting (Model 8550, AMP and OFS active)	CST	M1,CT0,T0,W1,H0,A0,L0,C0,D0,BUR 0002 #,RPT 1.00 S, STA 1.000KHZ,STP 9.000KHZ,SWT1.00 S,MRK5.000 KHZ, FRQ 1.000KHZ,PLL 0DEG,TPH 0DEG,AMP 1.00V,OFS 0MV	
(Model 8551, AMP and OFS active)	CST	M1,CT0,T0,W1,H0,A0,L0,C0,D0,BUR 0002 #,RPT 1.00 S, LEE 10.0US,TRE 10.0US,TPH 0DEG,PLL 0DEG, FRQ 1.000KHZ,DTY 50%,WID 100US,AMP 1.00V,OFS 0MV	
Current Parameter Setting (Model 8550, HIL and LOL active)	CST	M1,CT0,T0,W1,H0,A0,L0,C0,D0,BUR 0002 #,RPT 1.00S, STA 1.000KHZ,STP 9.000KHZ,SWT 1.00S,MRK 5.000KHZ, FRQ 1.000KHZ,PLL 0DEG,TPH 0DEG,HIL 0.50V,LOL -0.50V	
(Model 8551, HIL and LOL active)	CST	M1,CT0,T0,W1,H0,A0,L0,C0,D0,BUR 0002#,RPT 1.00S, LEE 10.0US,TRE 10.0US,TPH 0DEG,PLL 0DEG, FRQ 1.000KHZ,DTY 50%,WID 100US,HIL 0.50V,LOL -0.50V	

Table 4-8. HP's Model 8116A - Mode/Parameter Messages (continued)

MESSAGE	MNEMONICS ASCII CODE	ASCII CODE DELIMITER	Description
HP-IB Universal Commands			
	DC4		Device clear (DCL)
	EOT		Selected device clear (SDC)
	BS		Group execute trigger
Interrogate Parameter			
	IERR		Interrogate error
	IFRQ		Interrogate frequency
	IDTY		Interrogate duty cycle
	IWID		Interrogate width
	IHIL		Interrogate high level
	ILOL		Interrogate low level
	IAMP		Interrogate amplitude
	IOFS		Interrogate offset
	IBUR		Interrogate burst
	IRPT		Interrogate repetition rate
	ISTA		Interrogate start frequency
	ISTP		Interrogate stop frequency
	IMRK		Interrogate marker frequency
	ISWT		Interrogate sweep time
Edge Control			(Model 8551 only. Not part of HP8116A commands set
	E0		Fastest edge transitions
	E1		Linear edge transitions
Error Reporting			
(Response to IERR)	NO ERROR		No error detected
	WAVEFORM ERROR		Not used in Model 8550/8551
	DUTY C. ERROR		Not used in Model 8550/8551
	WIDTH ERROR		Incompatible width and frequency setting
	TIMING ERROR		Incompatible burst and frequency setting
	HANDLING ERROR		Programming parameters with values outside their limits
	LEVEL ERROR		Programming amplitude levels with values outside their limits
	LIMIT ERROR		Same as LEVEL ERROR except HIL/ LOL window is active
HP-IB Status Byte			
(Response to SPOLL)	Bit 1		Timing error
	Bit 2		Programming Error
	Bit 3		Syntax Error
	Bit 4		System Failure (Not used in 8550/8551)
	Bit 5		Autovernier in process
	Bit 6		Sweep in process (Model 8550 only)
	Bit 7		Service request
	Bit 8		Buffer not empty (Not used in 8550/8551)

(*) Engineering notations can not be used in combination with delimiters. For example, the following command will result in an error message: FRQ 1.000E+3KHZ. Use either engineering notation or delimiters only. The following two examples are legal: FRQ 1.000E+6, or FRQ 1.000 MHZ.

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Maintenance & Performance Tests Section 5

5-1. INTRODUCTION

This section provides maintenance, service information, and performance tests for the models 8550 and 8551. Fuse replacement procedure, line voltage selection and disassembly procedure are also included.

WARNING

The procedures described in this section are for use only by qualified service personnel. Do not perform these procedures unless qualified to do so. Many of the steps covered in this section may expose the individual to potentially lethal voltages that could result in personal injury or death, if normal safety precautions are not observed.

5-2. LINE VOLTAGE SELECTION

The Model 8550 may be operated from either 115 Vac or 230 Vac nominal 50 - 60 Hz power sources. A special transformer may be installed for 100 Vac and 200 Vac ranges. The instrument was shipped from the factory set for an operating voltage of 230 Vac. To change the line voltage, proceed as follows:

WARNING

Disconnect the Model 8550 from the power cord and all other sources before changing the line voltage setting.

1. Using a flat-blade screwdriver, place the line voltage selection switch in the desired position. The selected voltage is marked on the selection switch.

2. Install a power line fuse consistent with the operating voltage. See paragraph 5.3

CAUTION

The correct fuse type must be used to maintain proper instrument protection.

5-3. FUSE REPLACEMENT

The Model 8550 has a line fuse to protect the instrument from excessive current. This fuse may be replaced by using the procedure described in the following:

WARNING

Disconnect the instrument from the power line and from other equipment before replacing the fuse.

1. Place the end of a flat-blade screwdriver into the slot in the LINE FUSE holder on the rear panel. Push in and rotate the fuse carrier the holder and its internal spring will push the fuse and the carrier out of the holder.

2. Remove the fuse and replace it with the proper type using Table 5-1 as a guide.

CAUTION

Do not use a fuse with a rating higher than specified or instrument damage may occur. If the instrument persistently blows fuses, a problem may exist within the instrument. If so, the problem must be rectified before continuing operation.

5-4. DISASSEMBLY INSTRUCTIONS

If it is necessary to troubleshoot the instrument or replace a component, use the following disassembly procedure to remove the top cover:

POWER LINE	RATING	FUSE TYPE
90 - 125V	1.0A, 250V	5x20mm/slo-blo
195 - 250V	0.5A, 250V	5x20mm/slo-blo

Table 5-1. Line Fuse Selection

1. Remove the two screws that secure the top cover to the rear panel.

2. Grasp the top cover at the rear and carefully lift it off the instrument. When the tabs at the front of the cover clear the front panel, the cover may be pulled completely clear.

3. When replacing the top cover, reverse the above procedure; be sure to install the tabs at the front panel before completely installing the cover.

5-5. SPECIAL HANDLING OF STATIC SENSITIVE DEVICES

MOS devices are designed to operate at a very high impedance levels for low power consumption. As a result, any normal static charge that builds up on your person or clothing may be sufficient to destroy these devices if they are not handled properly. When handling such devices, use precautions which are described in the following to avoid damaging them.

1. The MOS ICs should be transported and handled only in containers specially designed to prevent static build-up. Typically, these parts will be received in static-protected containers of plastic or foam. Keep these devices in their original containers until ready for installation.

2. Remove the devices from the protective containers only at a properly grounded work station. Also ground yourself with a suitable wrist strap.

3. Remove the devices only by the body; do not touch the pins.

4. Any printed circuit board into which the device is to be inserted must also be grounded to the bench or table.

5. Use only anti-static type solder sucker.

6. Use only grounded soldering irons.

7. Once the device is installed on the PC board, the device is normally adequately protected, and normal handling resume.

5-6. CLEANING

Model 8550 should be cleaned as often as operating condition require. Thoroughly clean the inside and the outside of the instrument. Remove dust from inaccessible areas with low pressure compressed air or vacuum cleaner. Use alcohol applied with a cleaning brush to remove accumulation of dirt or grease from connector contacts and component terminals.

Clean the exterior of the instrument and the front panel with a mild detergent mixed with water, applying the solution with a soft, lint-free cloth

5-7. REPAIR AND REPLACEMENT

Repair and replacement of electrical and mechanical parts must be accomplished with great care and caution. Printed circuit boards can become warped, cracked or burnt from excessive heat or mechanical stress. The following repair techniques are suggested to avoid inadvertent destruction or degradation of parts and assemblies.

Use ordinary 60/40 solder and 35 to 40 watt pencil type soldering iron on the circuit board. The tip of the iron should be clean and properly tinned for best heat transfer to the solder joint. A higher wattage soldering iron may separate the circuit from the base material. Keep the soldering iron in contact with the PC board for a minimum time to avoid damage to the components or printed conductors.

To desolder components use a commercial “solder sipper”, or better, solder removing SOLDER - WICK, size 3. Always replace a component with its exact duplicate as specified in the parts list.

5-8. PERFORMANCE CHECKS

The following performance checks verify proper operation of the instrument, and should normally be used:

1. As part of incoming inspection of instrument specifications;
2. As part of troubleshooting procedure;
3. After any repair or adjustment, before returning instrument to regular service.

5-8-1. Environmental Conditions

Tests should be performed under laboratory conditions having an ambient temperature of 25° ±5°C and a relative humidity of less than 8550%. If the instrument has been subjected to conditions outside these ranges, allow at least one additional hour for the instrument to stabilize before beginning the adjustment procedure. Always perform a self-calibration sequence before commencing with the performance checks. The self-calibration, if executed without any failure, ensures proper operation of the generator. If self-calibration failure was encountered, the instrument

first needs to be serviced, and the source of failure removed. Instructions how to self-calibrate the generator is given in paragraph 3-10.

5-8-2. Warm-Up Period

Most equipment is subject to at least a small amount of drift when it is first turned on. To ensure accuracy, turn on the power to the Model 8550 and allow it to warm-up for at least 30 minutes before beginning the performance tests procedure.

5-8-3. Front Panel Settings

To avoid confusion as to front panel settings, it is required that front panel set-up be reset to factory default values at the beginning of each of the performance tests. To reset front panel to factory default values depress **[2nd]** and then **[DCL]** push-buttons.

5-8-4. Recommended Test Equipment

Recommended test equipment for troubleshooting, calibration and performance checking is listed in table 5-2. Test instruments other than those listed may be used only if their specifications equal or exceed the required characteristics.

5-9. PERFORMANCE CHECKS PROCEDURE

5-9-1. Frequency Accuracy - Gated Mode

Accuracy specifications: ±3% of full scale up to 50.00MHz.
Equipment: Counter

1. Set 8550 as follows:

CONTROL	POSITION
Trigger Mode	Gated
Trigger Level	–10 V
Output	Squarewave

2. Set counter to frequency measurement.

3. Connect 8550 output to counter input. Set 8550 frequency and verify counter frequency reading as follows:

8550 SETTING	COUNTER READING
5.000 Hz	4.850 Hz - 5.150 Hz
50.00 Hz	48.50 Hz - 51.50 Hz
500.0 Hz	485.0 Hz - 515.0 Hz
5.000 KHz	4.850 KHz - 5.150 KHz
50.00 KHz	48.50 KHz - 51.50 KHz
500.0 KHz	485.0 KHz - 515.0 KHz
5.000 MHz	4.850 MHz - 5.150 MHz
10.00 MHz	9.700 MHz - 10.30 MHz
30.00 MHz	29.10 MHz - 30.90 MHz
50.00 MHz	48.50 MHz - 51.50 MHz

If model 8551 is tested, modify front panel FREQ setting to PER, and proceed with the next two tests.

8551 SETTING	COUNTER READING
999.9 ms	970.0 ms - 1.030 s
99.99 ms	97.00 ms - 103.0 ms

Table 5-2. Required Test Equipment.

Instrument	Recommended Model	Specifications	Use (*)
Counter	HP5334B	100MHz Universal	P,A,T
DMM	HP3478A	0.1V - 100Vac rms, DC	P,A,T
Pulse/Function Generator	Tabor 8551	1mHz - 20MHz	P
Synthesizer	Marconi 2019	80KHz - 1040MHz	P,A
DC power supply	Fluke 341A	0V - 30V 0.1%	P,A
Oscilloscope	Tek 2465B	400MHz band width	P,A,T
Distortion analyser	K-H 6900	100Hz - 1MHz	P,A
Spectrum analyser	HP 3588A	10KHz - 350MHz	P
Feedthrough Termination	Tek 011-0129-00	50Ω, 2W, 0.1%	P,A
20dB feedthrough Attenuator	Tek 011-0086-00	50Ω, 2W, 2%	P
AM detector	Wavetek-Datron D152	50Ω, 0.2 - 1000MHz	P

(*) P= Performance Test, A= Adjustments, T= Troubleshooting

5-9-2. Frequency Accuracy - Continuous Mode

Accuracy specifications: ±3% of full scale up to 999.9 mHz; ±0.1% of full scale from 1.000 Hz to 50.00 MHz (full scale reading is 5000 counts).
Equipment: Counter

1. Set 8550 as follows:

CONTROL	POSITION
Output	Squarewave

2. Set counter to frequency measurement.
3. Connect 8550 output to counter input. Set 8550 frequency and verify counter frequency reading as follows:

8550 SETTING	COUNTER READING
9.999 Hz	9.989 Hz - 10.01 Hz
99.99 Hz	99.89 Hz - 100.1 Hz
999.9 Hz	998.9 Hz - 1.001 KHz
9.999 KHz	9.989 KHz - 10.01 KHz
99.99 KHz	99.89 KHz - 100.1 KHz
999.9 KHz	998.9 KHz - 1.001 MHz
9.999 MHz	9.989 MHz - 10.01 MHz
10.00 MHz	9.999 MHz - 10.01 MHz
50.00 MHz	49.95 MHz - 50.05 MHz

5-9-3. Amplitude Accuracy

Accuracy specifications (1KHz): ±4% of reading from 10 mV to 16.0 V.
Equipment: DMM, 50Ω feedthrough termination.

1. Set 8550 as follows:

CONTROL	POSITION
Display Modify	AMPL

2. Set DMM to ACV measurements (RMS).
3. Connect 8550 output to DMM input. Terminate the output with a 50Ω feedthrough termination. Set amplitude and output waveform and verify DMM reading as follows:

8550 SETTING	DMM READING
Sinewave 16.0 V	5.431 V - 5.883 V
Triangle 16.0 V	4.439 V - 4.809 V
Square 16.0 V	7.680 V - 8.320 V
Sinewave 9.99 V	3.391 V - 3.673 V
Sinewave 3.00 V	1.018 V - 1.103 V
Sinewave 999mV	339.1mV - 367.3mV
Sinewave 99.9mV	33.91mV - 36.73mV

If model 8551 is tested, modify front panel settings as follows and proceed with the next two tests.

CONTROL	POSITION
Operating Mode	Pulse
Output Waveform	Square
Period	1600 µs
Pulse Width	800 µs
Transitions	Linear, 10 ns

8551 SETTING	DMM READING
Square 16.0 V	7.750 V - 8.250 V
Ramp 16.0 V	2.45 V - 2.70 V

5-9-4. DC Characteristics

Accuracy specifications: ±(1% of setting + 1% of amplitude + 2 mV), within ±8 V; ±(1% of setting + 1% of amplitude + 0.2 mV), within ±800 mV
Equipment: DMM, 50Ω feedthrough termination.

1. Set 8550 as follows:

CONTROL	POSITION
Amplitude	100 mV

2. Set DMM to DCV measurements.
3. Connect 8550 output to DMM input. Terminate the output with a 50Ω feedthrough termination. Set 8550 offset and verify DMM reading as follows:

OFFSET SETTING	DMM READING
±7.50 V	±7.422 V to ±7.578 V
±5.00 V	±4.947 V to ±5.053 V
±3.00 V	±2.967 V to ±3.033 V
±1.00 V	±0.987 V to ±1.013 V

4. Change 8550 amplitude setting to 10.0 mV. Set offset and verify DMM reading as follows:

OFFSET SETTING	DMM READING
±100mV	±98.7mV to ±101.3mV

5-9-5. Squarewave Characteristics

Specified transition time: 6 ns (10% to 90% of amplitude).
Specified aberration: <5% of amplitude.
Equipment: Oscilloscope, 20dB attenuator.

1. Set 8550 as follows:

CONTROL	POSITION
Frequency	1.000 MHz
Amplitude	10.0 V
Output	Squarewave

2. Connect 8550 output to the oscilloscope input. Use the 20 dB attenuator and set oscilloscope input impedance to 50Ω.
3. Set oscilloscope and verify that the rise and fall times are less than 6 ns. Verify that overshoot and undershoot are less than 5% of amplitude.

5-9-6. Sine Characteristics

Specified total harmonic distortion: <1% from 10.00mHz to 100 KHz.
Specified harmonic signals: >40 dB below the carrier level from 100 KHz to 2.000 MHz; >21 dB below the carrier level from 2.000 MHz to 50 MHz.
Equipment: Distortion Analyzer, Spectrum Analyzer, 50Ω feedthrough termination, 20dB attenuator.

1. Connect 8550 output to distortion analyzer input.
2. Set distortion analyzer to % distortion measurements, set 8550 frequency setting, and verify distortion reading as follows:

8550 SETTING	DISTORTION READING
10.00 Hz	<1%
100.0 Hz	<1%
1.000 KHz	<1%
10.00 KHz	<1%
100.0 KHz	<1%
1.000 MHz	<1%

3. Tune spectrum analyzer for minimum display amplitude, and adjust gain so that fundamental corresponds to 0 dB.
4. Change 8550 amplitude setting to 10.0 V.
5. Connect 8550 output to spectrum analyzer input through a 20dB feedthrough attenuator.
6. Set 8550 frequency setting and verify harmonic distortions levels as follows:

8550 SETTING	HARMONICS LEVEL
2.000 MHz	>40 dB
50.00 MHz	>21 dB

5-9-7. Sine Flatness

Level Flatness: ±2% to 9.999 MHz; –15% to 50.00 MHz.
Equipment: Oscilloscope.

1. Set 8550 as follows:

CONTROL	POSITION
Amplitude	1.20 V

2. Connect 8550 OUTPUT to the oscilloscope, set oscilloscope input impedance to 50Ω, and set oscilloscope to display the sinewave within exactly 6 vertical divisions.
3. Change 8550 Frequency setting to 9.999 MHz. Verify that peak to peak of the displayed sinewave is greater than 5.8 divisions.
4. Change 8550 Frequency setting to 50.00 MHz. Verify that peak to peak of the displayed sinewave is greater than 5.1 divisions.

5-9-8. External Trig, Gate, Burst Characteristics

Specifications: Triggered - Each positive going transition at the front panel TRIG IN connector stimulates the 8550 to generate one complete output waveform. **Gated -** External signal at the TRIG IN connector enables the 8550 output. Last cycle of output waveform always completed. **Burst -** Each positive going transition at the front panel TRIG IN connector stimulates the 8550 to generate a burst of preselected number of cycles.
Equipment: Pulse/function generator, oscilloscope.

5-9-8-1. External Trigger

1. Set 8550 as follows:

CONTROL	POSITION
Frequency	1.000 MHz
Trigger Mode	TRIG'D

2. Set external pulse/function generator period to 10μs and 4 V positive pulse and connect its output to the 8550 TRIG IN BNC connector. Set oscilloscope and verify on the oscilloscope that 8550 outputs a triggered signal. Leave external pulse generator connected to the 8550 for the next test.

5-9-8-2. External Gate

1. Set 8550 as follows:

CONTROL	POSITION
Frequency	1.000 MHz
Trigger Mode	GATED

2. Set oscilloscope and verify on the oscilloscope that 8550 outputs a gated signal. Leave external pulse generator connected to the 8550 for the next test.

5-9-8-3. External Burst

1. Set 8550 as follows:

CONTROL	POSITION
Frequency	1.000 MHz
Trigger Mode	BURST

2. Set oscilloscope and verify on the oscilloscope that 8550 outputs a burst of two complete output waveforms. Remove external pulse generator connection from the 8550 for the next test.

5-9-9. Internal Trigger, Burst Characteristics

Specifications: Triggered - An internal timer repeatedly generates a single output waveform. Burst - An internal timer repeatedly generates a burst of preselected number of cycles.
Equipment: Oscilloscope.

5-9-9-1. Internal Trigger

1. Set 8550 as follows:

CONTROL	POSITION
Frequency	10.00 KHz
Trigger Mode	TRIG'D
Int. Trig. Per.	1 ms

2. Set 8550 to Internal Trigger mode by depressing **[2nd]** and **[INT TRG]** push-buttons in sequence.
3. Set oscilloscope and verify on the oscilloscope that 8550 outputs repetitive triggered waveform.

5-9-9-2. Internal Burst

1. Set 8550 as follows:

CONTROL	POSITION
Frequency	10.00 KHz
Trigger Mode	Burst
Int. Trig. Per.	1 ms

2. Set 8550 to Internal Burst mode by depressing **[2nd]** and **[INT TRG]** push-buttons in sequence.
3. Set oscilloscope and verify on the oscilloscope that 8550 outputs repetitive bursts of two complete output waveforms.

5-9-10. Manual Trig, Gate, Burst Characteristics

Specifications: [MANUAL] push-button simulates external stimulant.
Equipment: Oscilloscope, universal counter/timer.

5-9-10-1. Manual Trigger

1. Set 8550 as follows:

CONTROL	POSITION
Frequency	10.00 Hz
Trigger Mode	TRIG'D

2. Connect 8550 output to the oscilloscope input. Set oscilloscope time base to 1 ms.
3. Depress a few times the **[MANUAL]** push-button and verify that you get a single sinewave waveform on the oscilloscope every time that the **[MANUAL]** push-button is depressed. Leave 8550 output connected to the oscilloscope for the next test.

5-9-10-2. Manual Gate

1. Set 8550 as follows:

CONTROL	POSITION
Frequency	10.00 KHz
Trigger Mode	GATED

2. Depress a few times the **[MANUAL]** push-button and verify that you get a gated sinewave waveform on the oscilloscope every time that the **[MANUAL]** push-button is depressed. Remove 8550 output from the oscilloscope for the next test.

5-9-10-3. Manual Burst

1. Set 8550 as follows:

CONTROL	POSITION
Frequency	10.00 MHz
Trigger Mode	BURST
Burst	4000

2. Connect 8550 output to the universal counter/timer input. Set counter to Totaling measurement mode. Reset counter.
3. Depress the **[MANUAL]** push-button once and verify that counter reading is exactly 4000 counts.

5-9-11. Trigger Start-Phase Offset Accuracy

Specifications: –90° to +90° ±3°, to 500 KHz.
Equipment: Oscilloscope.

1. Set 8550 as follows:

CONTROL	POSITION
Amplitude	1.2 V
Trigger Mode	TRIG'D
I. TRIG	ON
Int. Trig. Per.	5.00 ms

2. Connect 8550 output to the oscilloscope input, and set oscilloscope input impedance to 50Ω.
3. Set vertical sensitivity on the oscilloscope to 0.2V per division. Set oscilloscope time base and observe that the 8550 output is displayed within exactly 6 vertical divisions.
4. Change 8550 Start-Trigger Phase Offset to –90° and observe that the base-line is shifted to the bottom of the sinewave; creating an haversine waveform. Observe that the base line is at the –3 division line ±1 small grid lines.
5. Change 8550 Start-Trigger Phase Offset to +90° and observe that the base-line is shifted to the top of the sinewave; creating an inverted haversine waveform. Observe that the base line is at the +3 division line ±1 small grid lines.

5-9-12. Phase Lock Loop Characteristics

Accuracy specifications: ±3%,±3° of reading from 10Hz to 100.0 KHz.
Equipment: Counter, pulse/function generator, synthesizer, 50Ω feedthrough termination, 50Ω "T" BNC connector, regular "T" BNC connector.

1. Set 8550 as follows:

CONTROL	POSITION
Operation Mode	PLL
Output Waveform	Squarewave
Display Modify	P. Offset

2. Connect test set-up as described in Figure 5-1.
3. Set external pulse/function generator period to 100ms, and duty cycle to 50%.

4. Set counter to Phase A to B function, trigger level A and B to 1.00 V, slope A and slope B to negative.
5. Set 8550 PLL phase offset and verify the following accuracy requirements:

8550 SETTING	COUNTER PHASE READING
45°	40.7° - 49.3°
90°	84.3° - 95.7°
150°	145.2° - 154.8°
–45°	310.7° - 319.3°
–90°	264.3° - 275.7°
–150°	205.2° - 214.8°

6. Change 8550 PLL Phase Offset setting to 0°, and trigger level setting to 0.0 V.
7. Change counter function setting to Ratio A/B, Trigger level A and B settings to 0.00 V, and Input Impedance A and B to 50Ω.
8. Connect test set-up as described in Figure 5-2.
9. Set synthesizer frequency, and verify counter reading as follows:

2019 SETTING	COUNTER RATIO READING

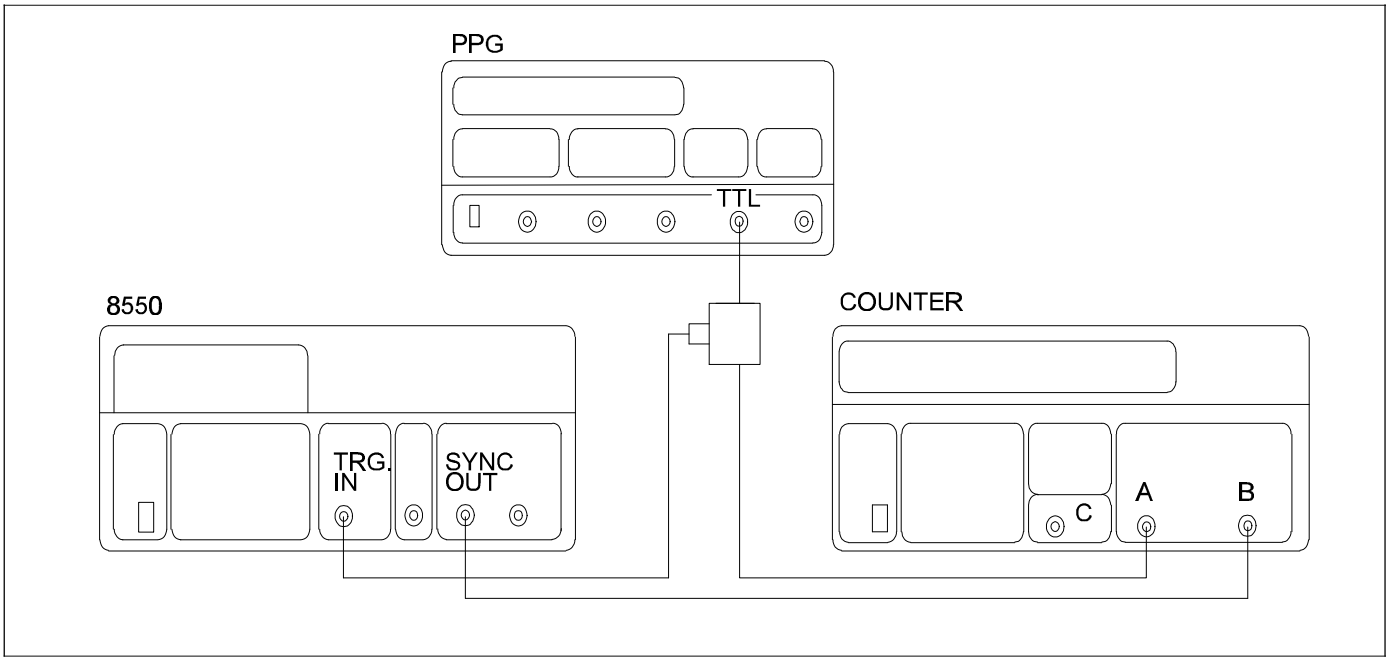
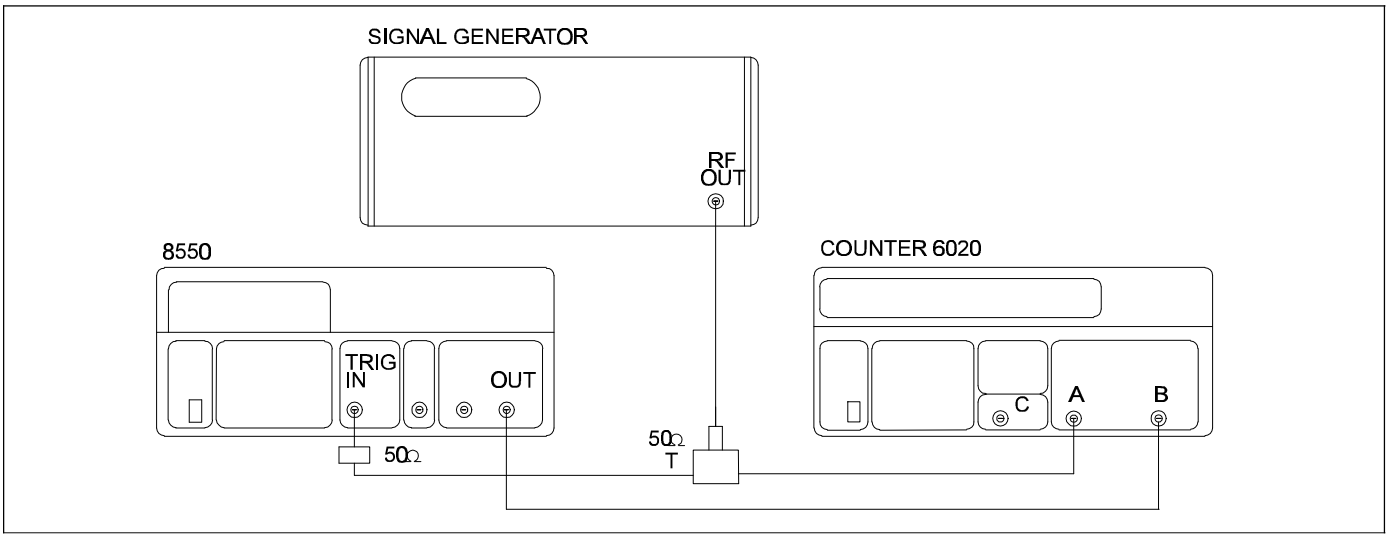


Figure 5-1. PLL Phase Offset Accuracy Check.

Figure 5-2. Phase Lock Loop Operation Check.



10.00000 MHz	1.0000000
20.00000 MHz	1.0000000
30.00000 MHz	1.0000000
40.00000 MHz	1.0000000
50.00000 MHz	1.0000000
60.00000 MHz	1.0000000

5-9-13. Amplitude Modulation Characteristics

Specifications: Envelop Distortion - <1% with carrier frequency <1.000 MHz; <3% with carrier frequency to 50.00 MHz.
Equipment: Pulse/function generator, distortion analyzer, AM detector .

1. Set 8550 as follows:

CONTROL	**POSITION**
MOD Mode	AM
Frequency	1 MHz
Amplitude	4 V

2. Connect test set-up as described in Figure 5-3.
3. Set external function generator frequency setting to 10.0 KHz, amplitude setting to 2.5 V, and offset setting to 1.25 V.
4. Verify that reading on the distortion analyzer is less than 1%.

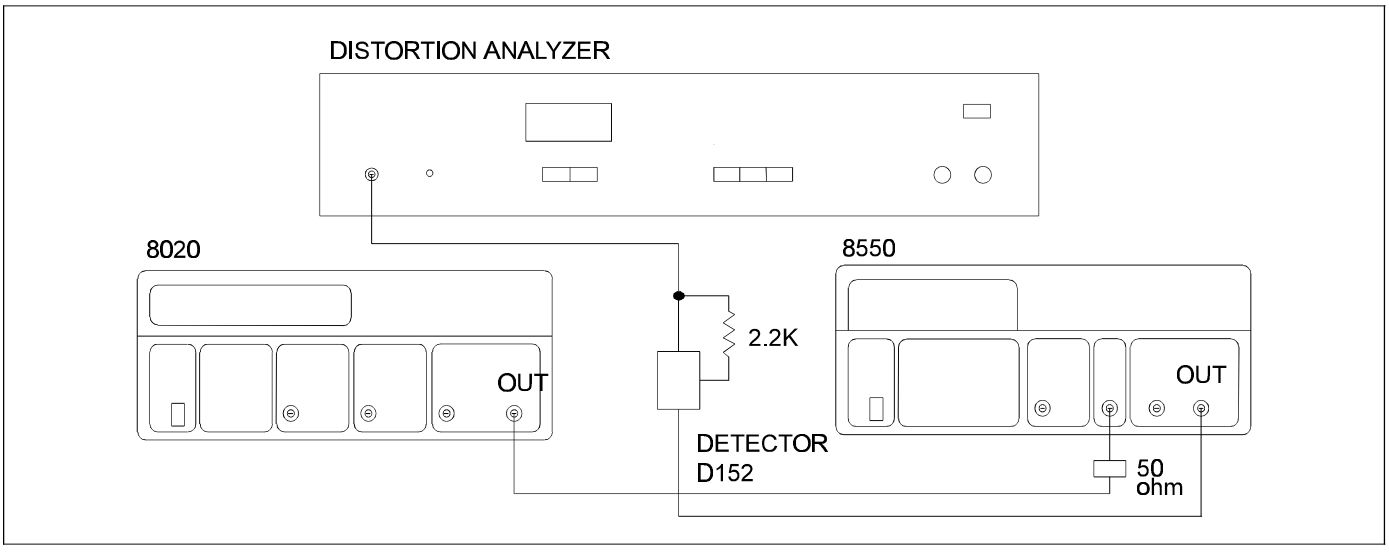


Figure 5-3. Amplitude Modulation Operation Check

5. Verify that reading on the distortion analyzer is less than 3% from 10.00 MHz to 50.00 MHz.

5-9-14. FM and VCO Characteristics

Specifications: VCO - 0 to –4.7 V, ±20% produces 1/1000 change from main frequency.
Equipment: Counter, DMM, dc power supply.
1. Set 8550 as follows:

CONTROL	POSITION
MOD Mode	FM
Frequency	999.9 KHz

2. Connect 8550 output to counter input and note frequency reading on the counter.
3. Connect dc power supply output to 8550 MOD input. Connect DMM leads to power supply output.
4. Vary power supply output voltage until the counter displays a frequency reading of 1.020 MHz. Verify that DMM reading is +1 V ±100 mV.
5. Change power supply leads polarity and vary power supply output voltage until the counter displays a frequency reading of 980.0 KHz. Verify that DMM reading is –1 V ±100 mV.
6. Change 8550 MOD Mode setting to VCO.
7. Vary power supply output voltage until the counter displays a frequency reading of approximately 1 KHz. Verify that DMM reading is –4.7 V ±500 mV.

5-9-15. Sweep Characteristics (model 8550)

Specifications: Logarithmic - 10 decades, Linear - 3 decades, Automatic up, down, up-down, and down-up directions. Gated, Triggered, and counted sweep
Equipment: Oscilloscope

1. Set 8550 as follows:

CONTROL	POSITION
Operating Mode	Linear Sweep
Sweep Direction	Down
Start Frequency	9.999 MHz
Stop Frequency	1.000 MHz
Marker frequency	5.000 MHz

2. Connect 8550 output connector to oscilloscope input. Set oscilloscope so that sweep may be observed. Note that 8550 sweeps down.
3. Modify 8550 sweep Time setting and observe that sweep time changes accordingly. Reset sweep time to 1 second.
4. Change sweep direction setting to UP and observe that 8550 sweeps up. Change sweep direction to up-down and watch the result.
5. Connect the rear panel Sweep Out BNC connector to oscilloscope and observe that DC level changes from 0 to 5V in approximately one second for a full sweep cycle.
6. Connect the rear panel Marker Out connector to the oscilloscope and observe that output changes from 0V to –5V when marker frequency is reached.
7. Change Operating Mode setting to Logarithmic Sweep and repeat the above tests.
8. Change 8550 Trigger Mode to Triggered. Observe that 8550 output sweeps once for every time that the [MANUAL] push-button is depressed.
9. Change 8550 Trigger Mode to Gated. Observe that 8550 output sweeps continuously as long as the [MANUAL] push-button is depressed.
10. Change 8550 Trigger Mode to Burst. Observe that 8550 output sweeps twice for every time that the [MANUAL] push-button is depressed. Change burst setting and observe that the number of sweeps corresponds to the number of selected burst count.

5-9-16. Pulse Width Accuracy (model 8551)

Accuracy Specifications: ±(5% + 2ns) from 10 ns to 99.9 ns; ±(4% +2ns) from 100 ns to 999 ms.
Equipment: Counter, Oscilloscope.

1. Set 8551 as follows:

CONTROL	POSITION
Operating Mode	Pulse
Output	Squarewave

2. Set counter to pulse width measurement and counter input impedance to 50Ω. Connect 8550 output to counter input.
3. Set 8551 Pulse Width and Period and verify counter reading as follows:

PERIOD SETTING	WIDTH SETTING	COUNTER READING
277.7 ns	50.0 ns	46.0 ns - 54.0 ns
277.7 ns	99.9 ns	93.0 ns - 107 ns
277.7 ns	100 ns	94.0 ns - 106 ns
1.500 µs	500 ns	478 ns - 522 ns
15.00 µs	5.00 µs	4.8550 µs
150.0 µs	50.0 µs	48.0 µs - 52.0 µs
1.500 ms	500 µs	480 µs - 520 µs
15.00 ms	5.00 ms	4.8550 ms
150.0 ms	50.0 ms	48.0 ms - 52.0 ms
1.500 s	500 ms	480 ms - 520 ms

4. Disconnect 8551 output from counter input and connect to oscilloscope input. Set oscilloscope input impedance to 50Ω.
5. Set 8551 Period to 100.0 ns and Pulse Width to 10.0 ns.
6. Verify that oscilloscope reading is between 8 ns to 12 ns.

5-9-17. Rise/Fall Time Accuracy (model 8551)

Accuracy Specifications: ±(5% + 2 ns) from 8 ns to 99.9 ms, ±(4% + 2 ns), above 99 ns.
Equipment: Counter, Oscilloscope, 50Ω feedthrough termination.

1. Set 8551 as follows:

CONTROL	POSITION
Operating Mode	Pulse
Output	Squarewave
Amplitude	4.00 V
Transitions	Linear

2. Set counter to Rise/Fall Time measurement. Connect 8551 output to counter input through the 50Ω feedthrough termination.
3. Set 8551 Period, Pulse Width, and Lead/Trail Transition times and verify counter reading as given in Table 5-3.

PERIOD SETTING	WIDTH SETTING	LEAD/TRAIL SETTING	COUNTER READING
1.000 µs	500 ns	99 ns	93.0 ns - 107.0 ns
2.000 µs	1.00 µs	500 ns	478 ns - 522 ns
20.00 µs	10.0 µs	5.00 µs	4.8550 µs - 5.20 µs
200.0 µs	100 µs	50.0 µs	48.0 µs - 52.0 µs
2.000 ms	1.00 ms	500 µs	480 µs - 520 µs
20.00 ms	10.0 ms	5.00 ms	4.8550 ms - 5.20 ms
200.0 ms	100 ms	50.0 ms	48.0 ms - 52.0 ms

Table 5-3. Rise/Fall Time Accuracy Tests

4. Disconnect 8551 output from the counter and connect to oscilloscope input. Set oscilloscope input impedance to 50Ω.
5. Change 8551 Period setting to 100.0 ns, Pulse width setting to 50.0 ns, and Lead and Trail setting to 10.0 ns.
6. Verify that oscilloscope reading is between 9.0 ns to 11.0 ns.

5-9-18. PWM Characteristics (model 8551)

Specifications: 0 to 5 V ±20% produces >10% pulse width change, from DC to 700 KHz.
Equipment: Counter, DMM, dc power supply.

1. Set 8551 as follows:

CONTROL	POSITION
MOD Mode	PWM
Operating Mode	Pulse
Period	1.500 ms
Pulse Width	500 µs
Output	Squarewave

2. Connect 8551 output to counter input. Set counter and note pulse width reading on the counter.
3. Connect dc power supply output to the 8551 MOD input. Connect DMM leads in parallel to power supply output.
4. Vary power supply output voltage until the counter displays a pulse width reading variance of 10%. Verify that DMM reading is between 4 V to 6 Vdc.

Theory of Operation Section 6

6-1. INTRODUCTION

This section contains an overall functional description of the 8550 series function generators as well as detailed circuit analysis of the various sections of the instruments. Information pertaining to the pulse width, the amplitude modulation and the standard IEEE interface are also included.

Information is arranged to provide a description of individual functional circuit blocks. As an aid to understanding, the descriptions are keyed to a block diagram and to Detailed schematics and component layout drawings which are located at the end of this instructions manual.

6-2. OVERALL FUNCTIONAL DESCRIPTION

The Model 8550/8551 is fully programmable function generator having various standard output functions. All parameters are adjustable through front panel touch switches or through IEEE programming. The high performance of the Model 8550/8551 is accomplished by utilizing a very fast, discrete analog circuits. Microprocessor and digital circuits control the performance of the analog circuits and permit direct interfacing to the front panel keyboard and display and to the GPIB. Figure 6-1 is a block diagram of the most important sections of the Model 8550/8551. Refer to this block diagram throughout the following general description.

The heart of the function generator is its VCO, where two identical currents with opposite polarities are created. These two currents are switched in, on and off, charging and consequently discharging a capacitor. This cycle generates a continuous ascending and descending voltage ramps. The repetition rate depends on the applied capacitor and the supplied current. The output of the VCO also generates a rectangular waveform.

The same ramp is used for driving the triangle and buffer. The triangle waveform is also utilized in generating the sinewave output by using a sine shaper. The three basic waveforms are then amplified or attenuated through the output amplifier and fed to the output connector. The output amplifier circuit is capable of driving its output waveforms into a 50Ω load.

The analog signals are controlled by D to A converters. The D to A converters receive their controlling information through serial to parallel converters; directed by the microprocessor components.

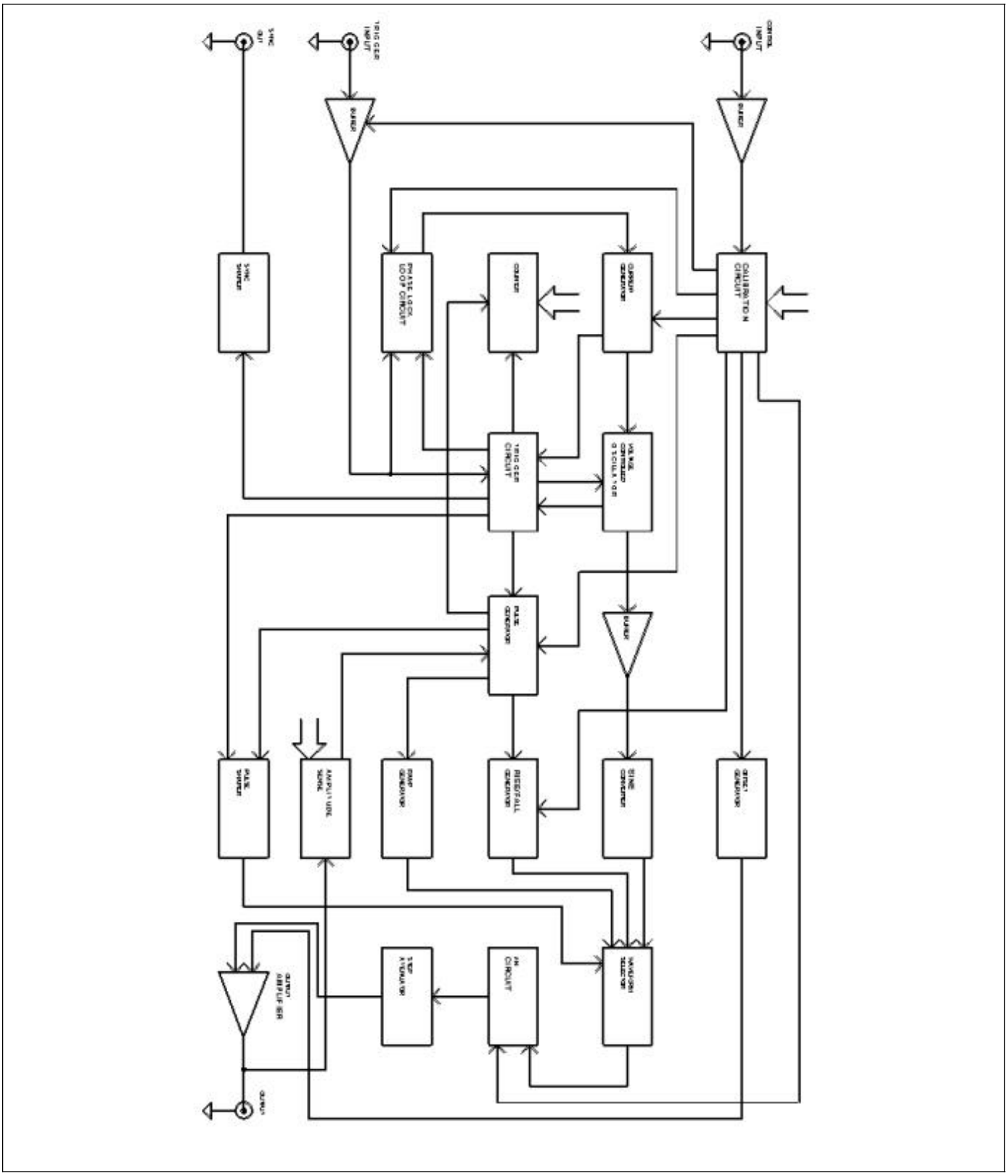
Model 8550/8551 is mechanically constructed on a number of plug-in boards. Each board contains different electronic circuits; making it easy for troubleshooting and servicing. Model 8550/8551 has four plug-in boards: CPU board, VCO board, Calibration board, Output Amplifier board, and Main board. Model 8551 has one additional pulse width and rise/fall time control board. The power supplies to the various sections of the generator is built on the main board assembly together with the connections for the plug-in boards. The various circuits on each board are described in the following.

6-3. C.P.U. BOARD

Model 8550/8551 operation is supervised by an internal microprocessor (CPU). The CPU controls parameter selection process, front panel switching, the displayed read-out and IEEE operation. All of these tasks are performed under software supervision. This section briefly describes the operation of the various sections of the microprocessor and its associated digital circuitry. For more complete circuit details refer to the schematics at the end of this manual.

Circuit operation centers around the microprocessor unit (CPU) U5. The CPU is an 8-bit microprocessor capable of directly addressing up to 64K bytes of program memory (ROM) and up to another 2K bytes of data memory (RAM). The microprocessor works with a 12 MHz clock which is divided by U6 to provide clocks for the various sections of the instrument. Software for the CPU is contained in one EPROM U8 containing 64K bytes of memory

Figure 6-1. Model 8550/8551 - Simplified Block Diagram



space. Temporary storage is provided by RAM U9 which can store up to 2K bytes of information.

6-3-1. Display and Keyboard Interface

Interfacing between the CPU, the keyboard and the display is performed by the Keyboard/Display interface U2. The information for the seven segment LEDs is sent through buffer U1 and limiting resistors RN1. U1 multiplex the digits and LED and drive the high current transistors Q1 through Q8 which, in turn, drive the anodes of the appropriate LED. The sense lines S0, S1 and S2 determine which of the front panel push-button were depressed.

6-3-2. Counter Circuit

The counter circuit is employed in the Model 8550/8551 for the purpose of controlling the accuracy of the frequency at the output connector. The counter circuit is composed of U10, U11, U13, and U14. The counter circuit counts the number of pulses from the VCO during a pre-determined gate time interval. The CPU then computes the relation between these pulses to the reference clock. The result is compared to the required accuracy. If deviation is sensed, the CPU sends correcting data to the current generator circuit.

6-3-3. IEEE-488 Interface Bus (GPIB)

The instrument has a built in IEEE-488 interface bus that permits remote control through a system controller. The IEEE interface is made of U15, (General Purpose Interface Adapter), U16 and U17 interface bus drivers. On the CPU side of the GPIB, data transmission is handled much like any other bus transaction. The output of the U15 is standard GPIB format and is buffered by the two GPIB drivers U16 and U17. The bus divers are necessary for enhancing the drive capability of the interface. Up to 15 devices may be connected in parallel.

6-4. V.C.O. BOARD

The following paragraphs contain descriptions of the various circuit that are available on the VCO board. The circuits that are discussed here are: the voltage controlled oscillator and the clamp circuit, the current generator circuit, the timing capacitors and the capacitance multiplier circuit, the sine shaper circuit, the trigger circuit, the SYNC out circuit, and the auxiliary circuits. Complete and detailed schematics of this board are located at the end of this manual.

6-4-1. Voltage Controlled Oscillator

The VCO is comprised of a comparator - U13, FET buffer - Q12, current switches - Q13, Q14, Q19, and Q20, and timing (range) capacitors - C21 through C24 and C36, and their associated components. The timing capacitors are charged by a positive constant current source which is made of Q18 and U18; creating a positive going linear voltage ramp which is applied to the positive input of U13.

When this ramp meets the +1.2 V reference voltage level which is applied to the negative input of the comparator, the current switch which is made of Q19 and Q20 reverses the polarity of the current which is applied to the timing capacitor; discharging the timing capacitor and creating a negative going linear voltage ramp.

At this time, the reference voltage at the negative input of the comparator is switched to -1.2 V by the current switch which is made of Q13 and Q14. When the negative going ramp meets the -1.2 V reference voltage level, the current switch reverses the polarity again. This sequence is automatically repeated; creating a triangular waveform.

The above triangular waveform is buffered by an impedance converter - Q12 ant its associated components and applied to the rest of the circuits through K1. This buffer isolates the timing capacitors from the level comparator and provides sufficient current drive for the level detector. The triangular waveform may be clamped at any voltage level between +1.2 V and -1.2 V for the purpose of generating start phase offsets. This is done by applying a programmable level at the cathode of CR10 diode. This programmable level is generated by circuits located on the calibration board and is applied through Q28, CR13, U29a, Q33, and Q23 through Q25. When the timing capacitor is clamped, the current source which is made of Q27, R114, and R121 injects positive current into CR13 - equal in magnitude to the current injected into CR10.

6-4-2. Current Generator

The current generator generates the necessary currents for the VCO and the trigger circuits. The current magnitude determines the oscillation frequency within a selected range. The frequency reference circuit which is located on the calibration board produces a voltage level which is applied to the VCO through J2 pin 13. This voltage is proportional to the frequency. This voltage is then converted to alternating positive

and negative currents by U15a, Q22, U18, Q18, U17, and Q21.

The calibration board also produces a voltage level which determines the amplitude of the triangular waveform in the VCO circuit. This voltage is applied to the VCO board through J2 pin 15. On lower frequencies, the amplitude of the triangular waveform is ±1.2 V. On higher frequencies, this level is reduced proportionally to compensate for delays in the VCO components.

6-4-3. Range Capacitors and Multiplier

The frequency at the main output is being generated by charging range capacitors with alternating currents from the current generator. The range capacitors C36, and C21 through C24 are used for the 100 Hz to 50 MHz ranges. They are connected to the VCO circuit through the relay K2. They are switched in and out of the circuit by the transistors Q8 through Q11.

The capacitor multiplier is used for the 10 mHz to 99.99 Hz ranges. The function of this circuit is to generate an equivalent large capacitance. The larger values of capacitors are required to generate lower frequencies. The capacitor multiplier is formed by U1 ,U2, U3, and their associated components. The multiplier ratio is selected by changing the ranging resistors in the negative feedback path of U1.

6-4-4. Sine Shaper

The sine shaper consists of a series of differential stages which are formed by limiting amplifier arrays U9, U11 and U12. The differential stages are connected in parallel and receive the drive signal from the triangle buffer output - U10. This circuit takes advantage of the non-linear characteristics of the transistors and by biasing them to different dc levels, the output of the common collector is shaped to a sinewave. The sinewave is then routed through R51 to an amplifier, amplified, and re-biased, to oscillate around 0 V, with a differential amplifier which is formed by Q2 through Q7 and their associated components. Q1 is an electronic switch which removes the supplied current from the sine amplifier when it is not being used.

6-4-5. Trigger and Burst Circuit

The trigger circuit is active when one of the trigger modes is selected. It provides 4 different trigger modes for the Model 8550/8551: continuous mode, triggered mode, gated mode, and counted burst mode. Refer to the schematic diagrams at the end of this manual throughout the following description. Detailed description of the various trigger modes is provided in the following paragraphs. The trigger command is applied to the trigger circuit from the calibration board through J2 pin 12 to the gates in U23b, U23c, and U23d. These gates shape and differentiate this signal and apply it to the reset input of U16a, and U16b.

Continuous Mode. In this mode, U16a is always set to its reset position. Its output control the emitter coupled transistors Q24 and Q25 through diodes CR11 and CR12. The current from R104 flows through Q24; producing a positive voltage on the collector of Q24 which is then applied through the emitter follower - Q23 to the cathode of the clamping diode CR10. CR10 is then negative-biased and does not interfere with the VCO oscillations.

Triggered Mode. In this mode, the reset input to U16a is released. The “D” input is kept at logic level “1" by Q26. A positive transition from the comparator U13, at the clock input to U16a, sets U16a output to logic level ”1" causing Q24 to turn off and forward biasing CR10 through the emitter follower Q23; clamping the triangle waveform to a certain voltage level. A positive going transition of the triggering signal is differentiated by U23, R118, and C46 and applied to the reset input of U16a; changing its state and reverse biasing diode CR10. then, the positive going charging current which was flowing through CR10 is diverted to the timing capacitor; allowing the VCO to oscillate until the next positive transition at the output of U13. This new transition sets U16a back to logic level “1" and clamps the VCO to a non-oscillating status.

Gated Mode. Gated mode operation is very much similar to the triggered mode operation except that a stable gating level is applied to the reset input of U16a. As long as the reset level is set to logic level “1", the VCO oscillates. When the reset level is set to logic level ”0", The VCO stops its oscillation after the last waveform is completed.

Burst Mode. In this mode, the differentiated triggering signal is applied to reset input of both U16a and U16b. Q26 no longer keeps the “D” input of U16a at a logic level “1". U16a output is at logic level ”1" and the VCO does not oscillate.

A trigger signal resets U16a and U16b enables the VCO, however, because the “D” input of U16a is now set to logic level “0", the pulses from the VCO cannot set U16a to logic level ”1" and cannot interrupt the VCO oscillation. The VCO pulses are then routed through the gate U21c to the burst counter which is made of U19, U20, and U22 and to the gates U21a and U21b. In parallel, the VCO pulses are applied to the clock input of U16b. When the burst counter reaches its maximum possible count (FFF) the next VCO positive going transition sets the “Q” output of U16b to logic level “1"; creating conditions for U16a to be set to logic level ”1" and to stop the VCO oscillation.

6-4-6. SYNC Output Circuit

The SYNC output generates a fixed voltage level signal, having a sharp and defined transitions, which are synchronous with the positive transitions at the main output connector. The signal from the VCO circuit is routed to the SYNC amplifier circuit via a selector U27a, U27b, and U27c. In continuous mode, the SYNC signal is taken from the VCO circuit; in gated and triggered modes the signal is shaped and taken from the trigger input signal; in burst mode the SYNC signal is taken from the burst circuit, with duration equal to the burst length. The SYNC signal is then coupled through U27d to the SYNC amplifier which is made of Q29 through Q32 and their associated components.

6-4-7. Auxiliary Circuits

The information for the various gates and digital controls is received from the CPU board in a form of serial data. The serial data is then converted to parallel data and is latched for constant control of the various circuits. U4 and U6 are used for TTL serial to parallel conversion; U24 and U25 are used for ECL serial to parallel conversion. TTL signals are converted to ECL by U26a, U26b, and U26d. U7 is a high power buffer which drives the various relays throughout the board. The timing capacitors are switched in and out by U5.

6-5. CALIBRATION BOARD

The following paragraphs contain descriptions of the various circuit that are available on the Calibration board. The circuits that are discussed here are: the reference circuit, the D/A control circuit, the Trigger input circuit, the phase lock circuit, and the counter conditioning circuit. Complete and detailed schematics of this board are located at the end of this manual.

6-5-1. Reference Circuit

The reference circuit provides accurate and controlled voltage references for adjusting and calibrating the various parameters of the instrument. The reference voltages are applied to the reference inputs of the various digital to analog converters. The octal DAC - U1, operational amplifiers U3, and U4 provide correcting voltages for the digital to analog converters. Operational amplifiers - U5 and U2 combine these correcting voltages with the +5 V and the -5 V references. External controls are applied to U5 through U8 and the analog multiplexer switch U7.

The output of U5b controls the reference input to the frequency D/A converter; the output of U5c controls the reference input to the amplitude D/A converter; the output of U5d controls the reference input to the pulse width D/A converter; the output of U2a controls the PLL phase-offset; and the output of U2b controls the trigger start phase offset.

6-5-2. D/A Parameter Control Circuit

The following describes the control circuits for the various parameters that are available for modification through front panel programming.

The offset parameter is controlled by a digital to analog converter U24, operational amplifiers U23 and U29, analog switch U25a, and their associated components. The digital to analog converter receives its digital commands from serial to parallel converters U27 and U28.

The frequency parameter is controlled by two digital to analog converters U6 and U14, operational amplifiers U9, U10, and U13, by transistor Q2, and their associated components. The current through the collector of Q2 controls the current generator in the VCO board.

Below 1 MHz, the amplitude of the triangle which is generated in the VCO circuit is controlled by an operational amplifier U22 and resistors R38 and R39. The triangle is set to operate within +1.2 V and -1.2 V amplitude limits. In higher output frequencies, above the range of 1 MHz, due to internal circuit delays, this triangle amplitude presents tendencies to increase. Whitin the output frequency range of 1 MHz to 10 MHz, a digital to analog converter U16 compensates this effect by injecting correcting current at the input to U22 through an analog switch U25b and R42. Within the range of 10 MHz to 50 MHz, the correcting current is generated by the digital to

analog converter U16, and applied through an analog switch U25c, R43, and thermistor T1.

The Calibration board also contains some circuits pertaining to the sweep outputs. The sweep output voltage is generated by the digital to analog converter U19, operational amplifier U18a and their associated components. The marker output signal is generated by an operational amplifier U18b.

6-5-3. Trigger Input Circuit

The trigger input circuit receives external stimulating signal, shapes it, and adjusts the internal threshold amplitude to the required level. The external signal is received through the TRIG IN BNC connector and is routed through R40 to the comparator U26 and its associated components. CR1 and CR2 are used as protection against overloading the comparator input. The threshold level is generated by a digital to analog converter U1, operational amplifier U4b and their associated components.

6-5-4. Phase Locking Circuit

Model 8550/8551 is capable of locking on an external signal and automatically adjust itself to the frequency and the phase of the external signal. The various parts of the locking circuit are described in the following.

U37a, U37b, and U37c is a signal selector which selects the signal to be applied to the phase detector input. The square wave signal from the VCO is applied to the second input of the phase detector through U38a. The phase detector is comprised of a “D” flip-flops U33a and U33b, gate U37d and their associated components. The phase lock loop also include a “pump charge” generator which is made of current switches Q5 through Q8, current generators made of Q9 and Q10, and their associated components. The loop amplifier is made of operational amplifier U32. The phase locking filtering capacitor-resistor networks are selected by a multiple analog switch U30 which connects the required feedback network to the loop amplifier. The phase locking detector is comprised of a window comparator U31a, U31b, R87, R88, R89, and level shifter made of CR3 and R66.

6-5-5. Counter Conditioning Circuit

Model 8550/8551 employs a built-in counter which is used in a number of applications such as frequency accuracy control, automatic calibration, measure frequency of an external signal, and more. The counter circuit itself is located on the CPU board assembly, however, signal conditioning and routing to the counter from the different parts of the instrument is controlled by circuits on the calibration board. The various parts of the conditioning circuits are described in the following.

The counter input may receive its signal from a number of sources: from the trigger input, from the VCO, from the phase sensing circuit U38c and U34a, and from the pulse width board (Model 8551 only). The signal for the counter input is selected by a selector which is made of gates U39a, U39b, U39c, and U39d. Frequencies up to 1 MHz are routed directly to the counter input. U40 divides signals above 1 MHz by 10 to reduce maximum frequency that may reach the counter input to 5 MHz. The signals for the counter circuit are converted from ECL to TTL by a comparator U35.

6-6. OUTPUT AMPLIFIER BOARD

The following paragraphs contain descriptions of the various circuit that are available on the Output Amplifier board. The circuits that are discussed here are: the pulse shaper circuit, the waveform selector circuit, the amplitude modulator circuit, the step attenuator, the power amplifier, the offset and amplitude sensing circuit, and the rise time sensing circuit. Complete and detailed schematics of this board are located at the end of this manual.

6-6-1. Pulse Shaper Circuit

The purpose of the pulse shaper is to convert the signal from the level detector to pulses having very fast rise and fall times and with precise amplitude. The pulse shaper is located on the output amplifier assembly board.

The squarewave for the pulse shaper may come either from the VCO board or from the pulse width board (Model 8551 only). The signal is routed to the output amplifier board through the connector J2 pin 2. The squarewave signal is conditioned by the line receiver U6 and routed to the pulse shaper input. The pulse shaper consists of emitter coupled transistors Q2, Q3, Q4, and Q5 positive and negative current generators U5b, Q6, R11, U5a, Q7, R10, and level shifter made of diodes CR1 through CR4. When the generator is set to operate in squarewave function, the output of the pulse shaper, alternates between the positive current source and the negative current source.

6-6-2. Waveform Selector Circuit

Model 8550/8551 is capable of generating different waveforms at the output connector, such as, sine and triangular waveforms. The waveform selector circuit selects the necessary waveform to be applied to the output amplifier circuit. This circuit is comprised of a quad DMOS switch U1. Its output is controlled by comparators U3a, U3b, U3c, and U3d. The output of the waveform selector circuit is connected to the amplitude modulator circuit.

6-6-3. Amplitude Modulation Circuit

The amplitude modulation circuit serves two purposes. The first task is control the amplitude at the output connector, the second is to modulate the carrier signal which is generated by the Model 8550/8551 with an external modulating signal.

The amplitude modulator is made of an analog multiplier circuit U2, differential amplifier U9, and their associated components. One input of U2 receives the waveform from the waveform selector circuit, the second input receives either a dc level for amplitude control or an external signal for amplitude modulation. The amplitude level is controlled by a digital to analog converter U10, operational amplifier U7 and their associated components.

6-6-4. Step Attenuator Circuit

The signal from the amplitude modulator is attenuated with the step attenuator circuit before it is routed to the output amplifier section and then with a post attenuator before the signal is applied to the output connector. The step attenuator circuit is made of three sets of “phi” shaped resistors R50 through R58. The resistors are switched in and out of the attenuator with relays K1, K2, and K3. The post attenuator is a 20dB attenuator which is connected between output of the power amplifier and the output connector. This post attenuator is made of K5, R120, R121, and R125.

6-6-5. Power Amplifier Circuit

Refer to the schematics at the end of this manual throughout the following description. The output amplifier is a wideband current feedback type amplifier. The signal from the step attenuators is fed to the power amplifier through the emitter of transistors Q11 and Q12 which are connected in a cascadable fashion with Q10 and Q13 respectively. Q15 and Q16 are emitter followers that drive the gain stage made of Q17 and Q18. Q19 and Q20 buffer the amplified signal for the final class B amplifier stage which is made of power transistors Q21 through Q24.

Note that the power transistors are mounted on special heat sinks mounted on a bracket which is connected to the side support to remove the heat stress from these transistors. Q25 with R95 and R96 set the quiscent current for the power transistors.

The current feedback is extracted from the output through R104, R105, R78, and R79 and is fed to the input transistors Q11 and Q12. The input bias current of the power amplifier is compensated by an operational amplifier U14, a buffer made of Q8 and Q9, and their associated components.

The operational amplifier U15 and resistors R68, R69, R91, R92, R97, R98, R104, and R105 closes this feedback around the power amplifier and compensate for its offsets and dc gain errors. R91 trimmer resistor adjusts the low frequency gain to be equal with the high frequency gain.

6-6-6. Offset and Amplitude Sensing Circuit

Offsets and amplitudes within the power amplifier are monitored by special circuits which are capable of measuring and adjusting both parameters to be within the required specifications. The information from the sensing circuits is sent to the CPU board; it is stored in special correction tables, and is automatically applied to the output digital to analog converters for full accuracy operation. The power amplifier offset if sensed by the comparator U16b and is transferred to the CPU through CR12. The amplitude is sensed by U16a. This comparator circuit compares the peak amplitude against a precise dc reference of -2.5 V. The result is converted to TTL and sent to the CPU board to be used in amplitude calibration tables.

6-6-7. Rise Time Sensing Circuit (Model 8551)

Similar to the offset and amplitude sensing circuit, the rise/fall times are measured by a special circuit and converted to correcting information to be used by the CPU circuit. The rise/fall time sensing circuit is made of a dual comparator U17 and its associated components. It coverts the rise time to an equivalent pulse width to be measured by the counter. The results are then compared by the CPU circuit to reference values, and translated to correcting factors which are later being used for accuracy correction.

6-7. MAIN BOARD

The main board assembly contains the power supply, calibration references, reference digital to analog circuits, connectors for the plug-in boards and the interconnections between the various boards which are used on Models 8550 and Model 8551. The various parts that are laid on the main board are described in the following. Complete and detailed schematics of this board are located at the end of this manual.

6-7-1. Power Supply Circuit

Refer to the power supply schematic at the end of this manual for the following discussions. The power supply consists of a main power transformer, three bridge rectifiers, four integrated regulators, +5 V, and -5.2 V linear power supply. The LINE fuse and the Line Selector are accessible at the rear panel. The LINE VOLTAGE SELECT switch select 115V or 230V operation.

CR7 is used as a full-wave rectifier to provide a sufficient DC voltage for the -24 V and +24 V regulators U9 and U10 respectively. CR6 is used as a full-wave rectifier to provide a sufficient DC voltage for the +15 V and -15 V regulators U6 and U7 respectively. The +5 V linear power supply is made of power transistor Q9, control amplifier U8b, Q4, R25, R28, and overload protection Q5 and R26. The -5.2 V linear supply is made of power transistor Q8, control amplifier U8a, Q6, R26, R29, and overload protection Q7 and R27.

6-7-2. Reference Distribution Circuit

The reference distribution circuit is responsible for distributing the ⁄2.5 V and the ⁄5 V reference voltages throughout the instrument. The +5 V reference is made of U2, and it is being distributed by the quad operational amplifier U1 and its associated components.

6-7-3. Reference DACs Circuit

The reference digital to analog converters generate reference voltages for correcting and compensating accuracy errors on the power amplifier and on the pulse width boards. The digital to analog converter U4, operational amplifier U5 and their associated components generate an offset correcting voltage for the power amplifier circuit. The digital to analog converter U12, operational amplifier U13 and their associated components generate an offset correcting voltage for the rise/fall time circuit. The D/A converters receive their digital commands from serial to parallel converters U3 and U11.

6-8. PULSE GENERATOR CIRCUIT (Model 8551)

The pulse generator board has the necessary circuits for generating pulses and ramps with variable pulse width and variable rise and fall times. The pulse generator board is only installed on Model 8551. The following paragraphs contain descriptions of the various circuit that are available on the pulse generator board. The circuits that are discussed here are: the monostable multivibrator circuit, the pulse width current generator circuit, the ramp generator circuit, the transition times generator circuit, the transition times current generator circuit, and the auxiliary circuits. Complete and detailed schematics of this board are located at the end of this manual.

6-8-1. Monostable Multivibrator Circuit

The Monostable Multivibrator generates a pulse with a certain width every time that a trigger input signal is received. This circuit is made of “D” flip-flop U18a, U18b, timing capacitors, ramp buffer Q28, comparator U20, and their associated components. In the stable state, the output of U18b (pin 15) is set at about -0.8 V - equal to the voltage level on the selected timing capacitor. This voltage is applied through an impedance converter and buffer Q28 to the inverting input of U20. The non-inverting input of U20 is kept at a lower voltage level by a dc control circuit. The resulting voltage level at the output of the comparator output (pin 5) is “0" ECL level (-1.8 V). The timing capacitor discharging current flows from Q36 through the output of U18b pin 15.

The triggering signal for the multivibrator is received from the VCO board through J2 pin 12 and is routed to the clock input of U18a. U18a together with the delay circuit which is made of R70 and C23 generate narrow positive going pulses every time that a positive transition from the VCO signal is received. This pulse triggers U18b and diverts the discharging current from Q36 to the timing capacitor. The discharging current causes the voltage on the timing capacitor to drop linearly until the voltage level at the inverting input to the comparator equals the dc level at its non-inverting input. At this time, the output of the comparator changes its state to “1" ECL level (-0.8 V) and sets U18b forcing a charge current on the timing capacitor from the output of U18b. The comparator output then returns to its previous stable state of ”0" ECL level, and waits for the next triggering signal.

6-8-2. Pulse Width Current Generator Circuit

The current generator is controlled by a digital to analog converter U24 which receives its controlling signals from the CPU board and by an operational amplifier U23. The reference input to the digital to analog converter is supplied form the calibration board. The voltage which is generated by the D/A converter is converted to current by an operational amplifiers U22a and U22b, transistors Q36 and Q38, and their associated components. The amplitude of the ramp, which is generated by the monostable circuit, at the non-inverting input of the comparator U20 is controlled by an operational amplifier U27b and resistors R99 and R103. Transistors Q35, Q37, and Q39, operational amplifier U27a, and their associated components, compensate for temperature variations, and control the discharging current which generate the ramp.

6-8-3. Ramp Generator Circuit

The ramp generator circuit generates the ramp waveform which is then made available at the 8551 output connector. The negative going ramp waveform is derived from the monostable circuit by discharging a timing capacitor. This ramp is buffered by Q28 and routed to the ramp amplifier input U21. An offset correcting voltage is summed to the same input through R68 and additional compensating voltage through R84. The positive going ramp at the output of U21 is inverted by an operational amplifier U19 and resistors R64 and R65. The selection of positive or negative going ramp to the output amplifier board is made by a relay K2.

6-8-4. Transition Times Generator Circuit

The transition times generator control the rise and fall times of the generated pulses at the 8551 output connector. In general, the variable rise and fall times are generated by charging and discharging a selected timing capacitor with a known level of current; generating a positive and negative going linear voltage ramps. The currents for the transition times generator will be discussed in paragraph 6-8-5.

Emitter coupled current switches Q22, Q24, Q23, and Q25 alternately switch the required current to a selected timing capacitor C1, C2, C3, C9, and C10. This generates a positive and consequently negative voltage ramps on the capacitors. The positive going ramp is limited to +1.5 V by a circuit made of U1b, Q2, and their associated components. The negative going ramp is limited to –1.5 V by a circuit made of U1a, Q1, and their associated components. The ±1.5 voltage limits are referenced to the -5 V reference voltage on the main board.

The generated squarewave with its linear transition times is buffered by a dual FET circuit Q8 and buffer U5, and then routed to the appropriate input on the output amplifier board.

6-8-5. Transition Times Current Generator

As discussed above, the transition times current generator circuit generates the required current to charge the timing capacitors for the transition time ramps. The current generator is controlled by a digital to analog converters U8 and U11 which receives their controlling signals from the CPU board. The reference input to the digital to analog converters is supplied form operational amplifiers U2a and U2b and are referenced to the -5 V reference voltage on the main board. The voltage which is generated by the D/A converters is converted to positive and negative currents by quad operational amplifiers U6 and U7, transistors Q14 through Q21, and their associated components

6-8-6. Auxiliary Circuits

The information for the various gates and digital controls on the pulse generator board is received from the CPU board in a form of serial data. The serial data is then converted to parallel data by a train of serial to parallel converters U28, U26, U12, U13, U14, U9, and U4 and is latched for constant control of the various circuits. The timing capacitors for the pulse width ranges are switched in and out by switching transistors Q29 through Q34. The timing capacitors for the transition times ranges are switched in and out by switching transistors Q3, and Q5 through Q7. These switching transistors are driven by quad operational amplifiers U3, U15, and U17.

The gate selector made of U16c and U16d is responsible for selecting a waveform for the output amplifier section. Selection can be made from rectangular squarewave or variable pulse width squarewave. The gate selector U16a and U16b is responsible for routing the correct signal to the counter circuit. Selection for the counter is made between the variable pulse width signal which is being generated on this board and between the rise/fall time sensing circuit which is generated on the output board. The gate U10 selects from normal and inverted signals to be applied to the switching transistors in the transition times generator circuit.

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Adjustments & Troubleshooting Section 7

7-1. INTRODUCTION

This section contains information necessary to adjust and troubleshoot the 8550 function generator and the 8551 pulse/function generator.

WARNING

The procedures described in this section are for use only by qualified service personnel. Do not perform these procedures unless qualified to do so. Many of the steps covered in this section may expose the individual to potentially lethal voltages that could result in personal injury or death if normal safety precautions are not observed.

7-2. ADJUSTMENTS

7-2-1. Environmental Conditions

Adjustments should be performed under laboratory conditions having an ambient temperature of 24°, ± 5°C and a relative humidity of less than 70%. If the instrument has been subjected to conditions outside these ranges, allow at least one additional hour for the instrument to stabilize before beginning the adjustment procedure. Between adjustments, Always leave top cover on the unit to keep internal temperature as stable as possible.

7-2-2. Warm-Up Period

Most equipment is subject to at least a small amount of drift when it is first turned on. To ensure long-term calibration accuracy, turn on the power to the Model 8550/8551 and allow it to warm-up for at least 30 minutes before beginning the adjustment procedure.

7-2-3. Recommended Test Equipment

Recommended test equipment for calibration is listed in Table 5-2. Test instruments other than those listed may be used only if their specifications equal or exceed the required characteristics.

7-2-4. Adjustment Procedures

All adjustments are performed with the POWER switch ON. The top cover should be removed to allow access to test points and adjustments. Always perform a self-calibration sequence before starting the adjustment procedure. The self-calibration, if executed without any failure, ensures proper operation of the generator. If self-calibration failure was encountered, refer first to the troubleshooting instructions in this section to verify and rectify the source of this failure. Instructions how to self-calibrate the function generator is given in paragraph 3-10.

WARNING

Take special care to prevent contact with live circuits or power line area

Instrument	Recommended Model	Minimum Specifications
Counter	HP5334B	100MHz, universal counter
DMM	HP3478AA	0.1V - 500Vac rms, DC, 0.05%
Function generator	Wavetek model 90	Sine, square, 2mHz - 20MHz, 20Vp-p
Synthesizer	Marconi 2019	80KHz - 1040MHz, 1ppm
Oscilloscope	Tektronix 2465B	400MHz analog bandwidth
Distortion Analyzer	K-H 6900	10Hz - 1MHz, 0.01% resolution
20dB Attenuator	Tektronix 011-0086-00	50Ω, 2W, 2%

Table 7-1. Recommended Test Equipment

which could cause electrical shock resulting in serious injury or death. Use an isolated tool when making adjustments.

When necessary, refer to the component layouts in Section 9 for determining adjustment points. Follow the procedure in the sequence indicated because some of the adjustments are interrelated and dependent on the proceeding steps.

Verify that the generator is functioning according to the performance checks. Make sure that all results are within, or close to, the range of the required specifications, otherwise refer to the troubleshooting procedures given later in this section.

Perform the following adjustment procedure. If an adjustment can not be made to obtain a specific result, refer to the troubleshooting procedures.

NOTE

If not otherwise specified, before every adjustment set Model 8550/8551 controls to factory defaults by depressing **[2nd]** and **[DCL]** in sequence. Always connect the output BNC connector through a 50Ω feedthrough termination.

7-3. ADJUSTMENT PROCEDURE

7-3-1. Distortion Adjustment

Equipment: Distortion analyzer

1. Connect 8550/8551 output to distortion analyzer input as shown in Fuigure 7-1.
2. Adjust V.C.O. board trimmers R22 and R101 repeatedly, until the distortion reading on the analyzer is adjusted to minimum, but not more than 0.8%.

3. Change 8550/8551 setting to 9.999 KHz. Repeat step 2 for best distortion reading. Note that each one of these resistors contribute a small amount to the distortion correction. It is up to the service technician to find the most effective sequence to perform this step. Repeat steps 2 and 3 until distortion reading is equal and minimal in both frequencies.

7-3-2. Sine Level Adjustment

Equipment: DMM

1. Connect 8550/8551 output to DMM input as shown in Figure 7-2. Set DMM to DCV measurements and 200 mV range.

2. Adjust V.C.O. board trimmer R21 until DMM reading on is 0 V ±5 mV.

7-3-3. Squarewave Response Adjustment

Equipment: DMM, Oscilloscope (2465B), 20 dB feedthrough attenuator

1. Change 8550/8551 Frequency setting to 1.000 MHz, amplitude setting to 10.0 V, and output waveform to squarewave.

2. Connect 8550/8551 output through the 20dB attenuator to the oscilloscope input as shown in Figure 7-3. Set oscilloscope input impedance to 50Ω.

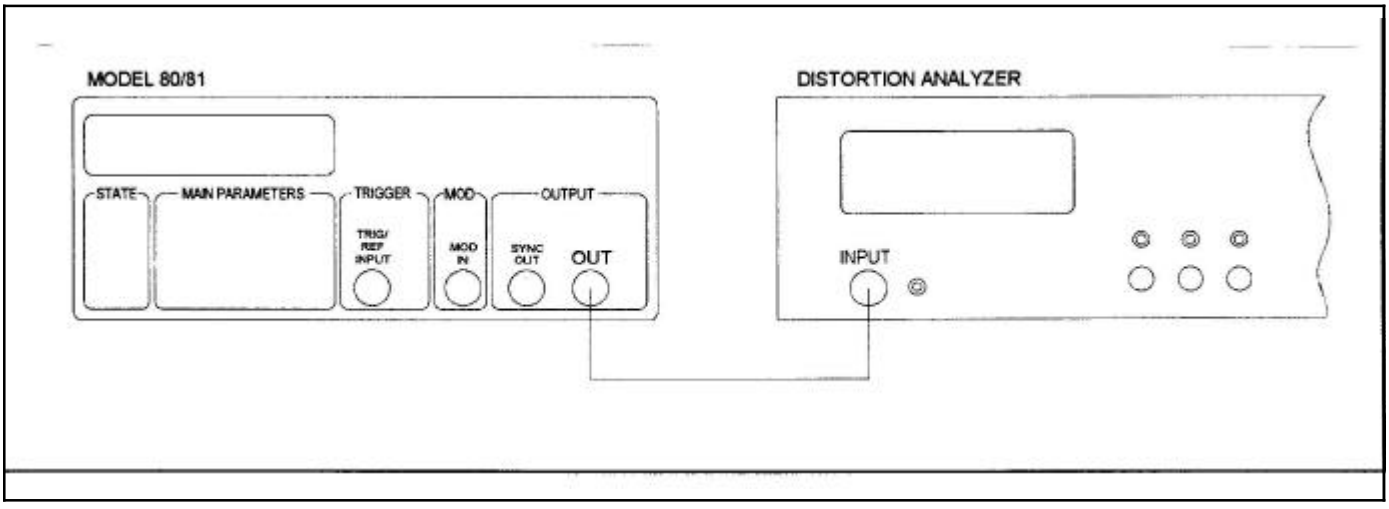
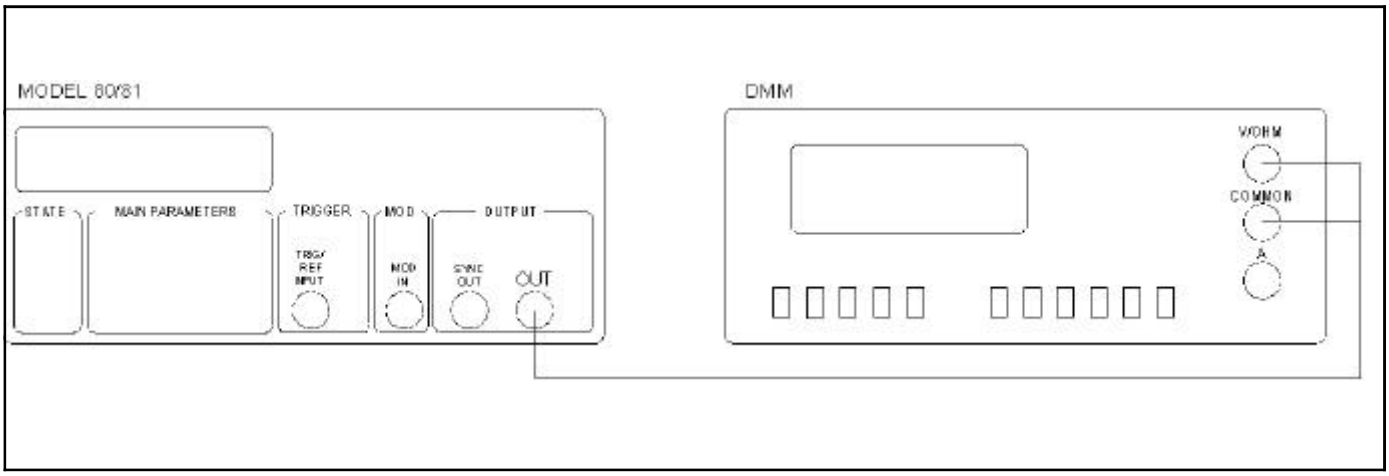


Figure 7-1. Connection - Distortion Adjustment.

Figure 7-2. Connection - Sine Level Adjustment.



3. Set oscilloscope vertical gain and time base, and adjust output board trimmer R84 for best pulse response.
4. Change 8550/8551 amplitude setting to 1.00 V. Set oscilloscope vertical gain and adjust output board trimmer R95 for best pulse response.
5. Repeat steps 4 and 5 until best pulse response is obtained in both adjustments.
6. Set DMM function to DCV and range to 2 V. Connect DMM leads across R93 and verify that DMM reading is less than 1.5 V, otherwise readjust R95.
7. Change 8550/8551 frequency setting to 10.00 KHz, amplitude setting to 10.0 V, and output waveform to squarewave.
8. Set oscilloscope vertical gain and time base, and adjust R91 for best pulse flatness.
9. Change 8550/8551 frequency setting to 1.000 KHz and readjust R91 for best flatness in this range.
10. Repeat steps 8 and 9 until best result is obtained in both steps.
11. Change Model 8550/8551 frequency setting to 50.00 MHz.
12. Set oscilloscope vertical gain and time base, and select R13 for best horizontal pulse symmetry.

7-3-4. Pulse Width Adjustment (Model 8551)

Equipment: Oscilloscope

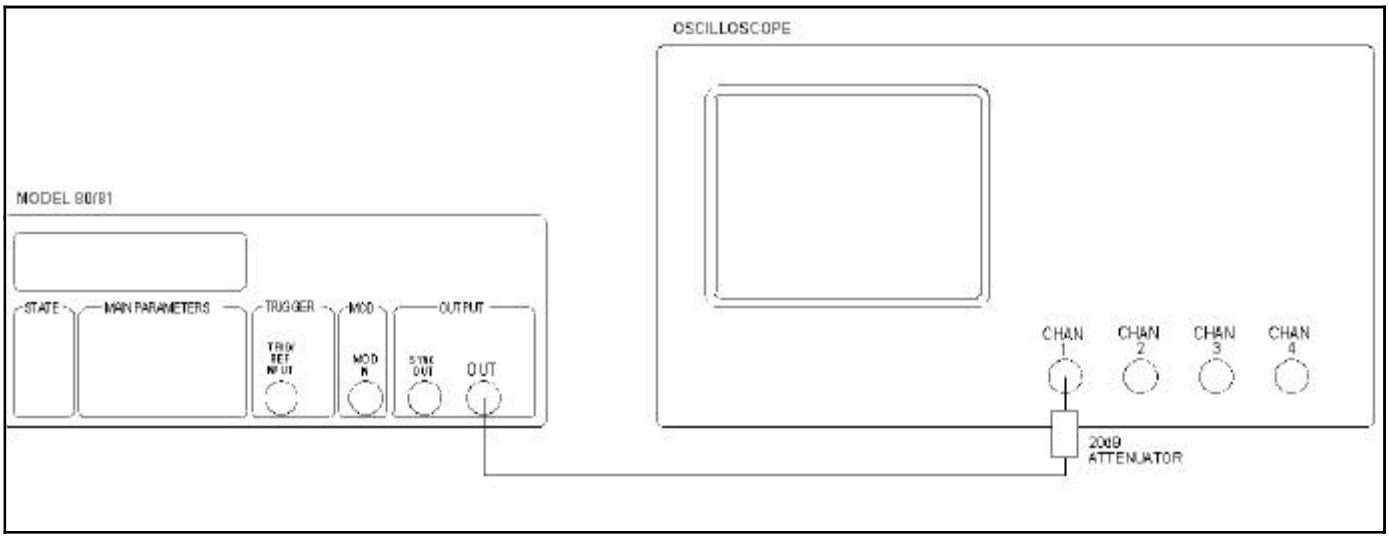
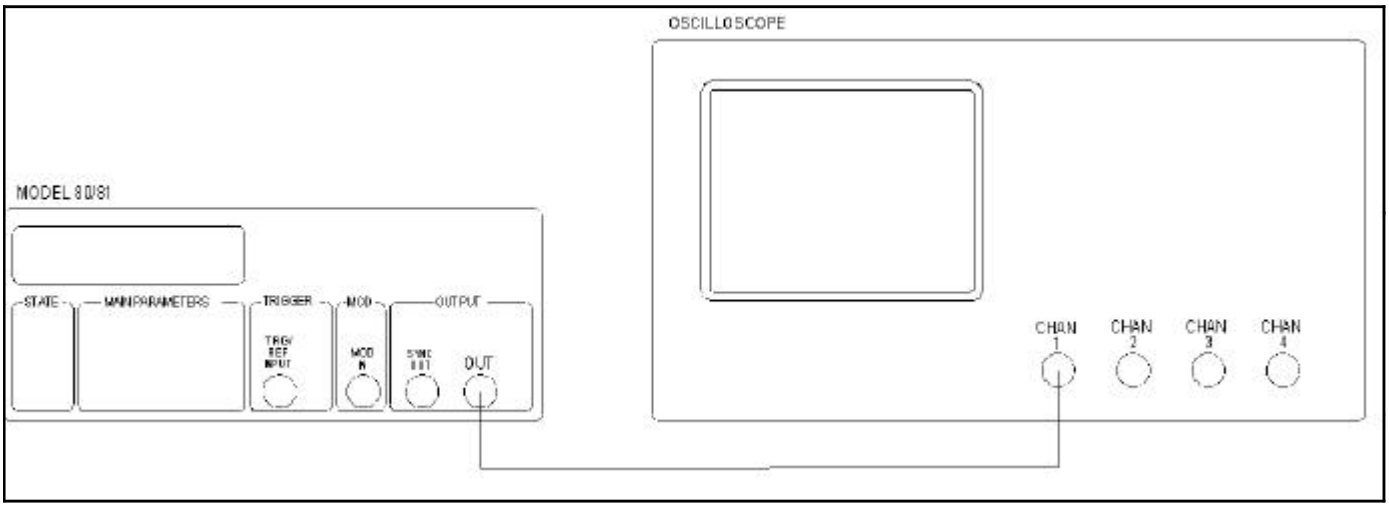


Figure 7-3. Connection - Squarewave Response Adjustment.

Figure 7-4. Connection - Pulsewidth/Ramp Adjustment.



1. Change 8551 operating mode setting to pulse mode, period to 100.0 ns, pulse width to 10.0 ns, and output waveform to squarewave.
2. Connect 8551 output to oscilloscope input as shown in Figure 7-4. Set oscilloscope input impedance setting to 50Ω.
3. Set oscilloscope vertical gain and time base, and adjust trimmer R100 on the pulse generator board to get a 10.0 ns ±1 ns reading on the oscilloscope.

7-3-5. Ramp Base-Line Adjustment (Model 8551)

Equipment: Oscilloscope

1. Leave Model 8551 connected to the oscilloscope as was shown in Figure 7-4. Change Model 8551 output setting to ramp.

2. Change oscilloscope input setting to DC coupling and 50Ω input impedance. Change oscilloscope vertical gain setting to be 100 mV/div. Adjust trace vertical position so that it appears exactly at the center line.
3. Connect 8551 output to the oscilloscope. Adjust R66 on the pulse generator board until the base line is calibrated on the center line.

7-3-6. Reference Oscillator Adjustment

Equipment: Synthesizer

1. Change 8550/8551 trigger level setting to 0.0 V.
2. Set synthesizer frequency to one of the following frequencies: 1 MHz, 5 MHz, or 10 MHz.

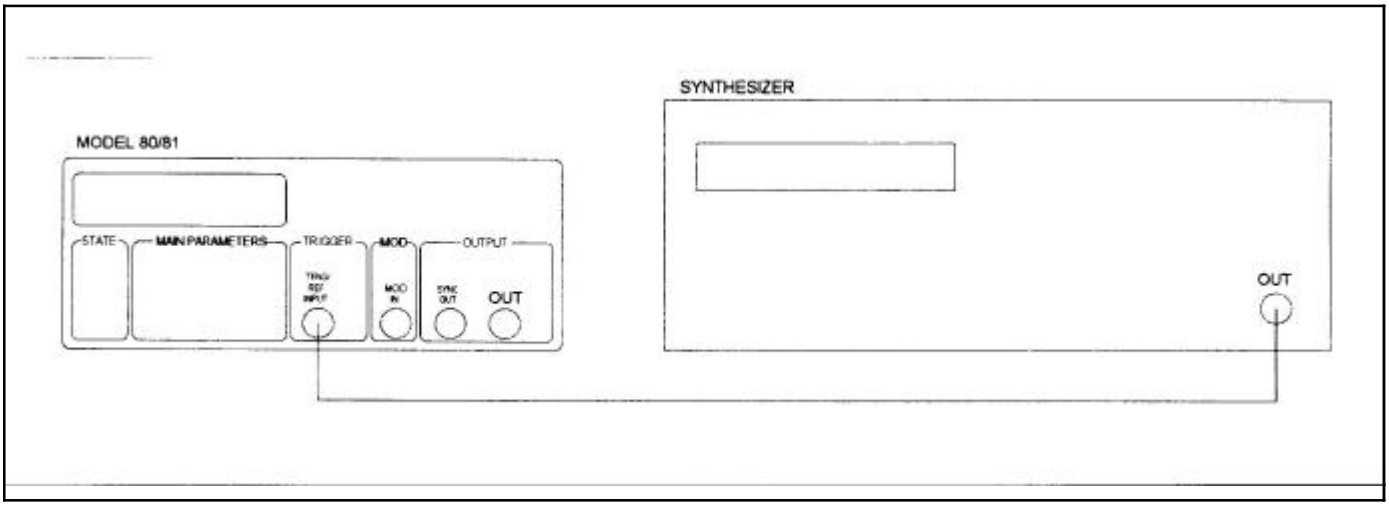


Figure 7-5. Connection - Reference Oscillator Adjustment.

Connect synthesizer output to 8550/8551 TRIG IN BNC connector.

4. Perform a self-calibration procedure as described in paragraph 3-10. Note that a leading + appears in front of the rotating bar; indicating that Model 8550/8551 accepted the external frequency reference as its new standard.

7-4. TROUBLESHOOTING

The troubleshooting instructions contained in this section are intended for qualified personnel having a basic understanding of analog, and digital circuitry. The individual should also be experienced at using typical test equipment as well as ordinary troubleshooting procedures. The information presented here has been written to assist in isolating a defective circuit, or circuit section; isolation of the specified component is left to the technician.

7-4-1. Recommended Test Equipment

The success or failure in troubleshooting a complex piece of equipment, like the Model 8550/8551, depends not only on the skills of the technician, but also relies heavily on accurate, reliable test equipment. Table 5-2 lists the recommended test equipment for a complete troubleshooting and adjustment of the Model 8550/8551. However, it is also possible to troubleshoot Model 8550/8551 with the minimum equipment which is listed in Table 7-1. Other equipment such as logic analyzer, and in-circuit emulator etc., could also be helpful in difficult situation.

7-4-2. Power-up tests

Upon power-up the Model 8550/8551 performs a set of tests which is described in paragraph 3-4. If the instrument locks up due to ROM or RAM fail, there is a little point in attempting to troubleshoot elsewhere unless the microcontroller circuit is operating properly.

7-5. TROUBLESHOOTING USING THE SELF-DIAGNOSTICS FUNCTION

An advanced feature of the Model 8550/8551 is its self-diagnostics capability. This feature helps in reducing troubleshooting time of faulty circuits to minimum. The self-diagnostics feature is a derivative of the self-calibration function. If, for whatever reason, the instrument can not calibrate itself to some built-in calibration limits, it automatically generates a failure list. This list can later be examined using front panel programming sequence. Calibration failures also produce error bits in the special calibration failure registers which are accessible through GPIB commands and queries.

Front panel calibration and self-diagnostics aspects are discussed in paragraphs 3-10 and 3-11. GPIB aspects of calibration failure status registers are discussed in paragraph 4-14-3. The self-calibration sequence may be initiated at any time. It is, however, recommended that such sequence be initiated under certain conditions which are listed in paragraph 3-10.

Troubleshooting procedure should also be initiated whenever the generator fails to perform either completely or partially. It is also required to troubleshoot Model 8550/8551 whenever the instrument fails to fully comply with its published specifications. In such cases, it is first recommended that self-calibration procedure be initiated. If this procedure has been completed without encountering an error, and if problem still remains, it is then necessary to remove the top and bottom covers and troubleshoot the generator using some other means. Note that the information given in the following do not intend to replace full scale troubleshooting, but merely to direct the service engineer to the area were the source of the trouble is located.

The self-diagnostics failure list is automatically generated after a self-calibration procedure. To initiate the self-calibration procedure depress the two front panel [AUTOCAL] push-buttons simultaneously, and observe that the generator displays the following message:

CAL?

The “?” (question mark) appears blinking; indicating that the instrument has not yet commenced with its calibration routine. Depress the [EXE] push-button and observe that the blinking question mark is replaced by a rotating LED bar. The bar rotates as long as the self-calibration program is in process.

If a calibration failure was detected, the generator displays the following message:

FAIL d

Where **d** represents a blinking digit in the range of 1 through 9. A function LED indicator, in the front panel MAIN PARAMETERS block, blinks simultaneously; indicating the source of the calibration failure. For example, **FREQ** indicator that blinks with a display reading of **FAIL 2** indicates that some circuits that generate the second frequency range failed to perform properly.

One may examine the full list of calibration failures immediately after a self-calibration program was executed, or at any later time provided, however, that the *CLS common command was not used before the list have been evaluated. To examine the full list of calibration failures immediately after a self-calibration program was executed depress the [FAIL LIST ⇑] or the [FAIL LIST ⇓] push-buttons. The following paragraphs describe each failure and give some ideas how to locate the source of the failure.

Whenever necessary, refer to the detailed schematic diagrams given in Section 9. The theory of operation section in this manual may also assist in understanding how the circuits should operate.

7-5-1. Frequency Calibration Failures

Failures in the frequency generation circuits are indicated by a blinking **FREQ** indicator with an associated displayed readout. In general, frequency failures may generate as a result of faults in the V.C.O., current generator, and the counter circuits. The following is a list of possible frequency calibration failures. Possible solutions to remove the source of these errors are suggested.

FAIL 1 - Check the capacitor multiplier circuit. Check K2, K3, and their driving circuit on the V.C.O. board.
FAIL 2 - Check capacitor multiplier circuit. Check K2, K3, and their driving circuit on the V.C.O. board.
FAIL 3 - Check C21, Q8, K2, K3, and their driving circuit on the V.C.O. board.
FAIL 4 - Check C22, Q9, K2, K3, and their driving circuit on the V.C.O. board.
FAIL 5 - Check C23, Q10, K2, K3, and their driving circuit on the V.C.O. board.
FAIL 6 - Check C24, Q11, K2, K3, and their driving circuit on the V.C.O. board.
FAIL 7 - Check C36 on the V.C.O. board. Check U16, U25 and their associated components on the calibration board.
FAIL 8 - Check C36, K3 and its drive on the V.C.O. board. Check U40, U16, U25, and their associated components on the calibration board.
FAIL 9 - Check U9 and its associated components on the calibration board.

7-5-2. Amplitude Calibration Failures

Failures in the amplitude generation circuits are indicated by a blinking **AMPL** indicator with an associated displayed readout. In general, amplitude failures may generate as a result of faults in the V.C.O., calibration, pulse width, and output amplifier boards. The following is a list of possible amplitude calibration failures. Possible solutions to remove the source of these errors are suggested. If **FAIL 1** through **FAIL 5** were detected refer first to the theory of operation section and verify proper operation of the following circuits: waveform Selector, amplitude modulator, step attenuator, output amplifier, and amplitude sensing circuits. For other failures proceed with the following list.

FAIL 1 - Check the sine generator and the sine amplifier circuits, check relay K1 and buffer U10 on the V.C.O. board.
FAIL 2 - Check relay K1 and buffer U10 on the V.C.O. board.
FAIL 3 - Check ECL signal on U23 pin 2 on the V.C.O. board.
Check ECL signal on U16 pin 2 on the V.C.O. board.
Check the pulse shaper circuit on the output amplifier board.
FAIL 4 - Check the pulse generator circuit on the pulse generator board.
Check the rise/fall time generator on the pulse generator board.
Check the output amplifier circuit on the output amplifier board.
FAIL 5 - Check U19, U21 and their associated components on the pulse generator board.

7-5-3. Offset Calibration Failures

Failures in the offset generation circuits are indicated by a blinking **OFST** indicator with an associated displayed readout. In general, offset failures may generate as a result of faults in the calibration, output amplifier, and main boards. The following is a list of possible offset calibration failures. Possible solutions to remove the source of these errors are suggested.

FAIL 1 - Check the offset compensation circuit U11, U12, U13, and their associated components on the main board.
Check the preamplifier circuit U9, resistor R38, and their associated components on the output amplifier board.
FAIL 2 - Check the offset generator circuit U23, U24, U29, and their associated components on the output amplifier board.

Check U8, Q14, R73, R82, and R83 on the output amplifier board.

7-5-4. Phase Lock Offset Calibration Failures

Failures in the phase locking circuits are indicated by a blinking P.OFST indicator with an associated displayed readout. In general, phase lock offset failures may generate as a result of faults in the calibration, and the CPU boards. The following is a list of possible phase lock offset calibration failures. Possible solutions to remove the source of these errors are suggested.

FAIL 1 - Check the signal selector circuit to the phase lock detector Uxx and its associating components on the calibration board.
Check the PLL detector Uxx on the calibration board
Check the trigger input circuit on the calibration board
Check the PLL filter U30, U32, and their associated components on the calibration board

FAIL 2 - Check the U3d, U4c, U2a, U38c, U34a, and their associated components on the calibration board.
Check the counter circuit on the C.P.U. board.

FAIL 3 - Check the components as in FAIL 2.

7-5-5. Trigger Phase Offset Calibration Failures

Failures in the trigger phase offset circuits are indicated by a blinking TRIG PHASE indicator with an associated displayed readout. In general, trigger phase offset failures may generate as a result of faults in the calibration, and the V.C.O. boards. The following is a list of possible trigger phase offset calibration failures. Possible solutions to remove the source of these errors are suggested.

FAIL 1 - Check the trigger input circuit U26 and its associated components. Also check the trigger phase offset control U2b, U3a, U3d, Q1, and their associated components on the calibration board.
Check the trigger logic circuit U23, U16, U21 and their associated components on the V.C.O. board

FAIL 2 - Check the trigger phase offset control circuit U2b, U3a, U3d, Q1, and their associated components. on the calibration board.

7-5-6. Counted Burst Calibration Failures

Failures in the counted burst circuit is indicated by a blinking TRIG BUR indicator with an associated displayed readout. In general, counted burst failures may generate as a result of faults in the V.C.O. board. The following is a list of possible counted burst calibration failures. Possible solutions to remove the source of these errors are suggested.

FAIL 1 - Check the counted burst circuit U19, U20, U21, U22, and their associated components on the V.C.O. board

7-5-7. Pulse Width Calibration Failures (Model 8551)

Failures in the pulse width circuit is indicated by a blinking WID indicator with an associated displayed readout. In general, pulse width failures may generate as a result of faults in the pulse generator board. The following is a list of possible pulse width calibration failures. Possible solutions to remove the source of these errors are suggested. If **FAIL 1** through **FAIL 8** were detected refer first to the theory of operation section and verify proper operation of the following circuits on the pulse generator board: monostable multivibrator, pulse width current generator, and auxiliary circuit.

Also verify proper operation of the pulse width reference control on the calibration board, and the counter circuit on the C.P.U. board. For other failures proceed with the following list. All of the following tests are performed on the pulse width board.

FAIL 1 - Check C22, R78, K3, U25, R87, R88 and their associated components.
FAIL 2 - Check U25, K3, and their associated components.
FAIL 3 - Check K3, check C33, Q32 and their driving circuit.
FAIL 4 - Check C34, Q29 and their driving circuit.
FAIL 5 - Check C35, Q33 and their driving circuit.
FAIL 6 - Check C32, Q31 and their driving circuit.
FAIL 7 - Check C37, Q30 and their driving circuit.
FAIL 8 - Check C36, Q34 and their driving circuit.

7-5-8. Rise/Fall Time Calibration Failures (Model 8551)

Failures in the rise/fall time circuit is indicated by a blinking LEAD or TRAIL indicator with an associated displayed readout. In general, rise/fall time failures may generate as a result of faults in the pulse generator or in the main boards. The following is a

list of possible rise/fall time calibration failures. Possible solutions to remove the source of these errors are suggested. If **FAIL 1** through **FAIL 6** were detected refer first to the theory of operation section and verify proper operation of the following circuits on the pulse generator board: rise/fall time current generator, rise/fall time generator, and rise/fall time output buffer on the pulse width board.

Also verify proper operation of the rise/fall time reference control on the main board. For other failures proceed with the following list. All of the following tests are performed on the pulse width board.

FAIL 1 - Check C10, K1, and their associated components.
FAIL 2 - Check C9, K1, Q7, and their associated components.
FAIL 3 - Check C4.
FAIL 4 - Check C3, Q6 and their driving circuit.
FAIL 5 - Check C2, Q3 and their driving circuit.
FAIL 6 - Check C1, Q5 and their driving circuit.

7-6. GENRAL TROUBLESHOOTING HINTS

The following troubleshooting procedures should be performed whenever the self-diagnostic routine is insufficient to identify the source of the fault. In some instances, for example, it will be impossible to execute a self-calibration routine because the generator either does not power up at all, the display is fully or partially blank, or front panel controls can not be modified because software-hardware related problem has locked the unit.

In such cases, it is recommended to first verify proper operation of the power supply circuit, the C.P.U. circuit, front panel display, and keyboard operation.

WARNING

The following procedures described in this section are for use only by qualified service personnel. Do not perform these procedures unless qualified to do so. The steps covered in the troubleshooting procedure may expose the individual to potentially lethal voltages that could result in personal injury or death, if normal safety precautions are not observed.

For in-circuit troubleshooting procedure, it is required to remove the top and bottom covers. With the above warning in mind, carfully remove the covers, and proceed with the following checks.

7-6-1. Power Supply Checks

It is highly suggested that the first step in troubleshooting the Model 8550/8551, as well as any similar equipment, would be to check the power supply. If the various supply voltages within the instrument are not within the required limits, troubleshooting the remaining circuits can be very difficult. Table 7-2 shows several checks that can be made to the power supplies within the generator. In addition to the normal voltage checks, it is also a good idea to check the various supplies with an oscilloscope to make sure that no noise or ringing is present.

In case of a “dead short” between one of the supplies to the common ground, it would be best to disconnect the entire supply section from the remaining of the circuitry, and then determine whether the problem is in the power supply or in the remaining circuits. Model 8550/8551 is equipped with such quick-disconnect points, which are located on the bottom side of the main PC board. To access these points, it is necessary to remove the bottom cover, and then to remove the solder layer from these points.

While troubleshooting the power supply section, bear in mind that the +15 V supply also provides

Test Point	Description	Test Result
+24 V	+24 V supply	+23 V to +25 V
–24 V	–24 V supply	–23 V to –25 V
+15 V	+15 V supply	+14.4 V to +15.6 V
–15 V	–15 V supply	–14.4 V to –15.6 V
+5 V	+5 V supply	+4.8 V to +5.2 V
–5.2 V	–5.2 V supply	–5 V to –5.4 V

Table 7-2. Power Supply Checks.

the reference voltage to the +5 V. Therefore, it would be impossible to troubleshoot the +5 V supply if the +15 V supply is defective. Similarly, the +5 V supply is used as a reference voltage to the -5.2 V supply.

7-6-2. Digital Circuitry and Display Checks

The most important section, to be verified after the power supply checks, is the digital section with its various clocks. Problems with the digital circuitry could cause erratic operation or erroneous display readings. Problems in the clock generator for the C.P.U. and the digital circuit may cause a complete malfunction of the entire section. The C.P.U. would not even start generating the control lines. This makes it impossible to troubleshoot the remaining of the circuits.

Check the various components, associated with the digital circuitry, clocks, and the IEEE-488 interface, using the information given in Table 7-3.

Test Point	Description	Test Result
U12 pin 13	CPU clock	10 MHz, TTL level signal
U6 pin 9	GPIB interface clock	5 MHz, TTL level signal
U6 pin 6	Display interface clock	1.25 MHz, TTL level signal
U6 pin 15	CPU timer clock	4.88 KHz, TTL level signal
U6 pin 1	Beeper clock	2.44 KHz, TTL level signal
U5 pin 30	ALE line	160ns, TTL level, positive going signal
U5 pin 29	PSEN line	265ns, TTL level, negative going signal
U5 pin 17	RD line	500ns, TTL level, negative going signal
U5 pin 16	WR line	500ns, TTL level, negative going signal
U14 pin 3	Accuracy control signal	1KHz, 50% duty cycle TTL level signal *
U14 pin 2	Control counter gate	Period=300ms, width=250ms, TTL signal *
U11 pin 1	10 MHz counter reference	10MHz, TTL level signal *
U11 pin 2	Counter synchronized gate	Period=300ms, width=50ms, TTL signal *
U4 pin 2	Strobe line	500ns, TTL, positive going signal §
U4 pin 12	Strobe line	500ns, TTL, positive going signal §
U4 pin 15	Strobe line	500ns, TTL, positive going signal §
U4 pin 4	Serial clock	500ns bursts, TTL, pos. going signal §
U5 pin 10	Serial data	TTL level bursts, positive going signal §
U2 pin 4	Keyboard interupt	30ms, TTL, positive going signal †

* Test results after selecting DCL.
§ Continuously depress one of the [x1 ⇑] or [x1 ⇓] vernier push-buttons.
† Depress and release once for each test.

Table 7-3. Digital Circuitry and Display Checks.

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Parts List Section 8

8.1 GENERAL

This section contains information for ordering replacement parts. the replacement parts are available from Tabor Electronics.

8.2 ORDERING INFORMATION

When ordering replacement parts, always include the following information:

a) Instrument Model number.
b) Instrument Serial number.
c) Tabor part number.
d) Part description.
e) Circuit designation (where applicable).
f) Vendor code number

8.3 VENDORS

A list of vendors, their address and their CAGE codes are given in Table 6-1.

8.4 PARTS DESCRIPTION

Table 8-2 lists parts that are used in Model 8551. Unless otherwise noted, resistance is given in Ω, ±5%, and capacitance is given in F, ±20%. Parts description in Table 8-2 overrides values shown on the schematic and the assembly drawings, in places where part description does not match.

Table 8-1. Model 8550/8551 - List of Vendors

Vendor	Address	CAGE Code
Amphenol Products	4300 Commerce Court, Lisle Illinois 60532	1CD05
Amphenol Canada	44 Metropolitan Road, Scaborough Ont M1R 2T9 Canada	03554
Analog Devices	One Technology Way, Norwood MA 06062	24355
AVX	Senaca Avenue, Olean NewYork 14760	96095
Belden Wire, Inc.	2200 U.S. highway, 27 South Richmond Indiana 47374	70903
Bourns Inc.	1200 Columbia Avenue Bldg. C, Riveside CA 92507	80294
Comlinear Corporation	4800 Wheaton Drive, Fort Collins Collorado 80525	62839
Corcom Inc.	1600 Winchester Road, Libertyville Illinois	05245
Cornell-Dubilier	150 Avenue L, Newark New Jersey 07101	14655
CTS Knights Division	400 Reidmann Avenue, Sandwich Illinois 60548	75378
Dale Electronics	2064 12th Avenue, Columbus Nebraska 68601	91637
E.F. Johnson Company	299 Johnson Avenue, Waseca Minnesota 56093	74970
General Instruments	600 West John Street, Hicksville New York 11802	14936
Hamlin	Lake/Grove Streets, Lake Mills Wisconsin 53551	12617
Harris Semiconductors	1301 Woody Burke Road, Melbourne Florida 32902	36472
HP (7 seg)	3000 Hanover Street, Palo Alto California 94304	50434
HP (Schottkey diodes)	3000 Hanover Street, Palo Alto California 94304	34649
Intel Corporation	3065 Bowers Avenue, Santa Clara California 95051	34649
International Resistor Co.	Greenway Road, Boone North Carolina 28607	74902
ITT Components	Holzhauser Strasse 62-32, D-1000 Berlin 72 Germany	
Kemet Elctronics Corp.	2835 Kemet Way, Simpson Ville South Carolina 29681	31433
Littlefuse	800 Northwest HWY, Des Plannes Illinois 60016	75915
LSI Computer Systems	1235 Walt Whitman Road, Melville New York 11747	55261

Table 8-1. Model 8551 - List of Vendors (continued)

Vendor	Address	CAGE Code
Maxim	120 San Gabriel Drive, Sunnyvale California 94086	1ES66
Molex	2222 Wellington Court, Lisle Illinois 60532	27264
Motorola	5006East McDowell Road, Phoenix Arizona 85008	04713
National Semiconductors	2900 Semiconductor Drive, Santa Clara California 95051	27D14
North American Philips Corp.	7158 Merchant Avenue, El Paso Texas 79915	59821
Projects Unlimited	3860 Wyse Road Dayton, Ohio 45414	04597
Seiko Instruments	2990 W. Lomita Blvd.	
SGS	1000 East Bell Road, Phoenix Arizona 85022	66958
SGS-Thompson Micro Elctr.	1310 Electronics Drive, Carrollton Texas 75006	5D590
Shurter AG	Werkhofstasse 8 CH-6002, Luzern Switzerland	61935
Signetics	811 East Argus Avenue, Sunnyvale California 94088	18324
Siliconix	2201 Laurelwood Road, Santa Clara California 95054	17856
Sprague Electronics	61 Split Brook Road STE 305, Nashua NH 3060	56289
Switchcraft Inc.	5555 N. Ellstone Avenue, Chicago IL 60630	82389
Takamisawa	18-7, Kamium-3 Chome, Setagaya-ku Tokyo 154, Japan	55101
Texas Instruments	13500N. Central Expressway, Dallas TX 75265	01295
TRW	14520 Aviation Blvd., Lawndale CA 90260	0128551
Wavetek-Datron	9045 Balboa Avenue, San Diego CA 92123	23338

Table 8-2. Model 8550/8551 - Parts List

Qty	Reference Designation	Description and Commercial Part Number	Tabor Part Number	Vendor Code
Current Generator Board Assembly			***6100-6210***	***23338***
1	C8	CAP CER 3.3P SR155C3R31MAA	1500-03R30	96095
1	C38	CAP CER 15P SR155C150MAA	1500-01500	96095
1	C20	CAP CER 470P SR155C471MAA	1500-04710	96095
1	C27	CAP CER 220P SR155C221MAA	1500-02210	96095
3	C16,C24,C39	CAP CER 10n SR155C103MAA	1500-01030	96095
1	C40	CAP CER 50n SR155C503MAA	1500-05000	96095
12	C10,C11,C15,C19,C21, C22, C23,C25,C28-C31	CAP CER 0.1µ SR155E104ZAA	1500-0104A	96095
2	C14,C18	CAP TANT 1.0µ T350A105M025AS	1540-01050	31439
12	C1-C7,C13,C17,C26, C36,C37	CAP TANT 10µ T350B106M025AS	1540-0106B	31433
1	C12	CAP ELEC 100µ 16V 2222.013	1532-0107P	59821
4	C32-C35	CAP ELEC 100µ 25V 2222.036	1533-01070	59821
2	CR1, CR2	DIODE HOT CARRIER 5082-2810	0300-10200	54893
1	CR3	DIODE ZENER 1N751A 5.1 V	0300-20010	14936
1	CR4	DIODE 1N4151	0300-00400	14936
3	J1-J3	CON FEMALE 2X8 90152-2216	3000-30520	27264
1	J4	CON RF MALE 131-1701-201	3000-16000	74970

Table 8-2. Model 8551 - Parts List (continued)

Qty	Reference Designation	Description and Commercial Part Number	Tabor Part Number	Vendor Code
1	L1	BEAD Ferrite CERAMAG24 57-1355	4200-00000	59821
1	Q1	TSTR J-309	0400-02510	17856
1	Q2	TSTR 2N5210	0400-01910	04713
4	Q3,Q4,Q9,Q10	TSTR PN3904	0400-01200	04713
4	Q5- Q8	TSTR 2N5179	0400-00700	04713
2	R61,R76	RES COMP 33 5% 1/4W	0100-03300	74902
2	R65,R102	RES COMP 82 5% 1/4W	0100-08200	74902
1	R48	RES COMP 100 5% 1/4W	0100-01010	74902
2	R64,R101	RES COMP 130 5% 1/4W	0100-01310	74902
1	R74	RES COMP 200 5% 1/4W	0100-02010	74902
1	R82	RES COMP 330 5% 1/4W	0100-03310	74902
4	R59,R60,R75,R77	RES COMP 470 5% 1/4W	0100-04710	74902
1	R9	RES COMP 510 5% 1/4W	0100-05110	74902
5	R50,R51,R83,R100,R109	RES COMP 560 5% 1/4W	0100-05610	74902
9	R79,R91,R92,R93,R94, R95,R78,R97,R98	RES COM 560 1/8W 5%	0102-05610	74902
4	R11, R49, R66,R111	RES COMP 1K 5% 1/4W	0100-01020	74902
1	R86	RES COMP 1.2K 5% 1/4W	0100-01220	74902
1	R10	RES COMP 1.5K 5% 1/4W	0100-01520	74902
6	R52,R62,R68,R85, R105,R108	RES COMP 1.8K 5% 1/4W	0100-01820	74902
6	R56,R63,R67,R84, R104,R107	RES COMP 2.7K 5% 1/4W	0100-02720	74902
1	R99	RES COMP 3.9K 5% 1/4W	0100-03920	74902
1	R72	RES COMP 4.7K 5% 1/4W	0100-04720	74902
3	R69-R71	RES COMP 6.8K 5% 1/4W	0100-06820	74902
1	R88	RES COMP 7.5K 1/8W 5%	0102-07520	74902
2	R87,R89	RES COMP 8.2K 1/8W 5%	0102-08220	74902
1	R90	RES COMP 10K 1/8W 5%	0102-01030	74902
7	R29,R30,R33,R47,R96, R103,R110	RES COMP 10K 5% 1/4W	0100-01030	74902
1	R31	RES COMP 100K 5% 1/4W	0100-01040	74902
1	R32	RES COMP 1M 5% 1/4W	0100-01050	74902
1	R36	RES MF 9.76 1% 1/4W	0104-9R760	74902
2	R57,R58	RES MF 499 1% 1/4W	0104-49900	74902
1	R17	RES MF 825 1% 1/4W	0104-82500	74902
1	R53	RES MF 1K 1% 1/4W	0104-10010	74902
1	R14	RES MF 2K 1% 1/4W	0104-20010	74902
3	R4,R7,R8	RES MF 3.32K 1% 1/4W	0104-33210	74902
1	R41	RES MF 3.92K 1% 1/4W	0104-39210	74902
2	R3,R13	RES MF 4.02K 1% 1/4W	0104-40210	74902
2	R73,R81	RES MF 4.99K 1% 1/4W	0104-49910	74902
1	R55	RES MF 5.62K 1% 1/4W	0104-56210	74902
1	R43	RES MF8.25K 1% 1/4W	0104-82510	74902
1	R54	RES MF 9.09K 1% 1/4W	0104-90910	74902

Table 8-2. Model 8551 - Parts List (continued)

Qty	Reference Designation	Description and Commercial Part Number	Tabor Part Number	Vendor Code
18	R6,R12,R15-16,R22, R24-28,R35,R37-40, R44-46	RES MF 10K 1% 1/4W	0104-10020	74902
1	R106	RES MF 12.5K 1% 1/4W	0104-12520	74902
1	R5	RES MF 20K 1% 1/4W	0104-20020	74902
2	R1,R42	RES MF 40.2K 1% 1/4W	0104-40220	74902
1	R80	RES MF 47.5K 1% 1/4W	0104-47520	74902
4	R2,R18,R19,R21	RES MF 49.9K 1% 1/4W	0104-49920	74902
2	R23,R34	RES MF 100K 1% 1/4W	0104-10030	74902
1	R20	RES MF 332K 1% 1/4W	0104-33230	74902
1	RN1	RES NET CSC-09A-01-103G 10K/9	0111-1103B	91637
2	RN2,RN3	RES NET CSC-03-08A 103G 10K/8	0110-01030	91637
2	RN4,RN5	RES NET CSC08A-03-182G 1.8K/8	0110-01820	91637
1	RN6	RES NET CSC09A-01-272G 2.7K/9	0111-1272B	91637
1	T1	RES 1K 5% TYPE 2322 642 63102	0114-01400	59821
1	U1	DAC AD7228AJN	0500-60200	24355
3	U2,U9,U18	DUAL OP AMP LM1458N	0500-56500	04713
2	U3,U4	QUAD OP AMPL LM324N	0500-53210	04713
1	U5	OP AMPL TL084CP	0500-56750	04713
1	U6	MAX 543ACP	0560-00850	1ES66
2	U7,U30	ANALOG SWITCH DG211CJ	0500-90900	17856
1	U10	OP AMP OP07CP	0500-56330	01295
8	U11,U12,U15,U20-21, U27-28,U36	8 BIT SHIFT REGISTER CD4094B	0540-01100	27014
4	U14,U16,U19,U24	D/A 10 BIT CONVERTER AD7533JN	0560-00700	1ES66
5	U13,U17,U22,U23,U29	OP AMP LM741N	0500-56310	04713
1	U25	ANALOG SWITCH DG411CJ	0500-91000	17856
1	U26	MAX9690ACPA	0500-60950	1ES66
1	U31	COMPARATOR LM393N	0500-53700	04713
2	U8,U32	BIMOS OP AMP CA3140E	0500-57200	36472
1	U33	ECL FLIP-FLOP MC10H131P	0500-45300	04713
1	U35	CMP05GP	0500-56360	24355
1	U37	ECL NOR MC10H102P	0500-45000	04713
2	U34,U39	ECL NOR MC10102P	0500-40900	04713
1	U38	ECL XOR/XNOR MC10107P	0500-40950	04713
1	U40	ECL DIVIDER MC10138P	0500-40930	04713
Front Panel Board Assembly			***6100-6191***	***23338***
1	C1	CAP ELEC 100µ 16V 2222.036	1532-01070	59821
2	C2,C3	CAP CER 0.1µ SR155C104ZAA	1500-01040	96095
4	DS1-DS4	7 SIGMENT LED HDSP 5601	1200-11000	50434

Table 8-2. Model 8551 - Parts List (continued)

Qty	Reference Designation	Description and Commercial Part Number	Tabor Part Number	Vendor Code
1	DS5	7 SEG LED HDSP 7801	1200-11100	50434
2	DS6	±1 LED HDSP 7807	1200-11200	50434
6	DS7,DS15,DS25,DS29, DS32,DS35	MINI 3MM LED RED HLMP1301	1000-00300	50434
29	DS8-14,DS16-24,DS26-DS28,DS30-31,DS33-34, DS36-S41	LED GRN MV 54124-A	1000-00900	14936
1	J1	FLAT CABLE 20 PIN 9L28020	6800-50600	10903
10	Q1-Q10	TSTR PNP 2N4403	0400-01800	04713
10	R1-R10	RES COMP 220 5% 1/4W	0100-02210	74902
2	R11-R12	RES COMP 10 5% 1/4W	0100-01000	74902
21	S1-S21	KEY SWITCH M320.03 E1-1	2000-61600	0128551
1	U1	IC 74LS42	0510-05300	04713
1	U2	IC 74LS138	0510-02700	04713
Main Board Assembly			***6100-6185***	***23338***
2	C1,C2	CAP ELEC 100µ 25V 2222.036	1533-01070	59821
2	C3,C4	CAP ELEC 3300µ 35V 2222.037	1534-03380	59821
2	C5,C6	CAP ELEC 1000µ 50V 2222.037	1535-01080	59821
2	C7,C8	CAP ELEC 10.000µ 16V 2222.037	1532-01090	59821
1	C9	CAP ELEC 1000µ 25V 2222.037	1533-01080	59821
2	C10,C11	CAP ELEC 100µ 16V 2222.036	1532-01070	59821
1	C13	CAP TANT 10µ 25V T351B106M025AS	1540-01060	31433
1	C14	CAP CER 1n SR155C102MAA	1500-01020	96095
3	CR1-CR3	DIODE 1N4151	0300-00400	14936
2	CR4-CR5	DIODE 1N5908	0300-90400	04713
2	CR6-CR7	DIODE BRIDGE W005	0300-50100	14936
2	CR8-CR9	DIODE BRIDGE KBU-6A	0300-50200	24936
5	Q1-Q4,Q7	TSTR PN3904	0400-01200	04713
2	Q5,Q6	TSTR PN3906	0400-01340	04713
1	Q8	TSTR MJE3055A	0400-40400	04713
1	Q9	TSTR MJE2955A	0400-40300	04713
2	R33,R27	RES COMP 0.27 5% 2W	0103-0R270	74902
2	R6,R8	RES COMP 2.7 5% 1/4W	0100-02R70	74902
1	R3,R25,R26	RES COMP 100 5% 1/4W	0100-01010	74902
4	R23,R24,R28,R29	RES COMP 1K 5% 1/4W	0100-01020	74902
1	R4	RES COMP 1.5K 5% 1/4W	0100-01520	74902
2	R1,R15	RES COMP 1.8K 5% 1/4W	0100-01820	74902
1	R2	RES COMP 2.2K 5% 1/4W	0100-02220	74902
1	R5	RES COMP 27K 5% 1/4W	0100-02730	74902
1	R20	RES MF 4.64K 1% 1/4W	0104-46410	74902
3	R9,R14,R22	RES MF 4.99K 1% 1/4W	0104-49910	74902

Table 8-2. Model 8551 - Parts List (continued)

Qty	Reference Designation	Description and Commercial Part Number	Tabor Part Number	Vendor Code
1	R19	RES MF 8.66K 1% 1/4W	0104-86610	74902
7	R10-R13,R17,R21,R30	RES MF 10K 1% 1/4W	0104-10020	74902
4	R16,R18,R31,R32	RES MF 20K 1% 1/4W	0104-20020	74902
1	SP1	AUDIO TRANSDUCER AT-02	0900-01900	04597
1	S1	SW MAINS ON-OFF NE18-2U-EE	2000-10600	23338
1	U1	QUAD OP AMP LM324	0500-53210	04713
1	U2	VOLTAGE REFERENCE REF02CP	0530-00100	24355
2	U3,U11	8 BIT SHIFT REGISTER CD4094B	0540-01100	27014
2	U4,U12	D/A 10 BIT CONVERTER AD7533JN	0560-00700	1ES66
3	U5,U8,U13	DUAL OP AMP LM1458N	0500-56500	04713
1	U6	VOLTAGE REGULATOR MC7815CP	0500-52100	04713
1	U7	VOLTAGE REGULATOR MC7915CP	0500-52500	04713
1	U9	VOLTAGE REGULATOR MC7924CP	0500-52700	04713
1	U10	VOLTAGE REGULATOR MC7824CP	0500-52600	04713
Output Amplifier Board Assembly			***6100-6230***	***23338***
4	C1-C4	CAP ELECTR 100µ 25V 2222.036	1533-01070	59821
6	C6,C7,C13,C17,C31,C35	CAP CER 1n SR155C102MAA	1500-01020	96095
12	C5,C9,C12,C20,C21,C26, C27,C57,C58,C60,C61	CAP CHIP 0.1µ C0805A104Z5AC	1560-01040	31433
13	C8,C11,C15,C16,C18, C24,C25,C34,C43,C51, C59,C62,C63	CAP TANT 10µ T350B106M025AS	1540-0106B	31433
1	C14	CAP CER 10n SR155C103KAA	1500-01030	96095
17	C22-23,C28,C30,C32, C36,C38-40,C46-49, C52,C53,C54,C56	CAP CER 0.1µ SR155C104ZAA	1500-01040	96095
1	C29	CAP CER 6.8n SR155C682KAA	1500-06820	96095
1	C33	CAP MICA 51P CD15ED510J03	1510-05100	14665
2	C37,C42	CAP CER 33p SR155C330KAA	1500-03300	96095
1	C41	CAP CER 470P SR155C471KAA	1500-04710	96095
1	C45	CAP CER 3.3P SR155C3R3KAA	1500-03R30	96095
2	C44,C50	CAP ELECTR 220µ 50V 2222.036	1535-02270	59821
1	C55	SELECTED VALUE - TYP 1.5p		96095
1	C64	CAP CER 22P SR155C220KAA	1500-02200	96095
1	C65	CAP CER 10P SR155C100KAA	1500-01000	96095
2	CR1,CR4	1N747A 3.6V MATCHED	0300-20110	23338
2	CR2,CR3	1N753A 6.2V MATCHED	0300-20200	23338
5	CR6-CR8,CR10,CR11	DIODE 1N4151	0300-00400	14936
2	CR12,CR13	DIODE ZENER 1N751A 5.1V	0300-20010	14936
2	CR14,CR15	DIODE 1N752A 5.6V MATCHED	0300-20100	23338
2	CR16,CR17	DIODE ZENER 1N746A 3.3V	0300-20000	14936

Table 8-2. Model 8551 - Parts List (continued)

Qty	Reference Designation	Description and Commercial Part Number	Tabor Part Number	Vendor Code
2	J1,J2	CON FEMALE 2X8 90152-2216	3000-30520	27264
2	J3,J4	CON RF MALE131-1701-201	3000-16000	74970
5	K1-K5	RELAY RY-05WK-R10	0900-00700	55101
15	L1-L6,L9-L15,L17-L18	BEAD Ferrite CERAMAG24 57-1355	4200-00000	66958
4	Q1,Q7,Q8,Q25	TSTR PN3904	0400-01200	04713
2	Q4,Q5	TSTR 2N5179	0400-00700	04713
2	Q6,Q9	TSTR PN3906	0400-01340	04713
3	Q10,Q11,Q15	TSTR MPS3646	0400-00200	04713
5	Q2,Q3,Q12,Q13,Q16	TSTR MPS3640	0400-00100	04713
4	Q18,Q19,Q21,Q23	TSTR 2N3866A	0400-01610	04713
4	Q17,Q20,Q22,Q24	TSTR 2N5160A	0400-00800	04713
1	Q14	TSTR J-109	0400-02500	17856
1	R13	SEL (TYP 2.4K)		74902
2	R94,R99	RES COMP 4.7 5% 1/4W	0100-04R70	74902
2	R101,R108	RES COMP 10 5% 1W	0101-0100A	74902
1	R77	RES COMP 22 5% 1/4W	0100-02200	74902
1	R89	RES COMP 39 5% 1/4W	0100-03900	74902
2	R40,R41	RES COMP 68 5% 1/4W	0100-06800	74902
1	R124	RES COMP 82 5% 1/4W	0100-08200	74902
5	R11,R19,R21,R114,R116	RES COMP 100 5% 1/4W	0100-01010	74902
1	R18	RES COMP 130 5% 1/4W	0100-01310	74902
2	R68,R96	RES COMP 270 5% 1/4W	0100-02710	74902
1	R37	RES COMP 470 5% 1/4W	0100-04710	74902
2	R5,R39	RES COMP 510 5% 1/4W	0100-05110	74902
1	R15	RES COMP 560 5% 1/4W	0100-05610	74902
4	R12,R75,R109,R110	RES COMP 1K 5% 1/4W	0100-01020	74902
1	R14	RES COMP 2.2K 5% 1/4W	0100-02220	74902
6	R8,R9,R25-26,R111-112	RES COMP 3.3K 5% 1/4W	0100-03320	74902
1	R6	RES COMP 4.7K 5% 1/4W	0100-04720	74902
6	R59,R60,R61,R70-72	RES COMP 10K 5% 1/4W	0100-01030	74902
1	R74	RES COMP 100K 5% 1/4W	0100-01040	74902
4	R102,R103,R106,R107	RES MF 10 1% 1/4W	0104-10R00	74902
3	R29,R30,R51	RES MF 24.3 1% 1/4W	0104-24R30	74902
2	R85,R90	RES MF 33.2 1/4W 1%	0104-33R20	74902
2	R1,R42	RES MF 49.9 1%	0104-49R90	74902
3	R56,R58,R125	RES MF 61.9 1%	0104-61R90	74902
1	R120	RES MF 61.9 1% 1W	0104-61R9B	74902
3	R27,R28,R54	RES MF 71.5 % 1/4W	0104-71R50	74902
2	R93,R100	RES MF 71.5 1/2W 1%	0104-71R5A	74902
2	R53,R55	RES MF 95.3 1/4W 1%	0104-95R30	74902
4	R62,R65,R117,R118	RES MF 100 1% 1/4W	0104-10000	74902
2	R122,R123	RES MF 100 .1% 1/4W	0105-10000	74902
2	R76,R80	RES MF 121 1/4W 1%	0104-12100	74902
2	R50,R52	RES MF 215 1% 1/4W	0104-21500	74902

Table 8-2. Model 8551 - Parts List (continued)

Qty	Reference Designation	Description and Commercial Part Number	Tabor Part Number	Vendor Code
2	R57,R121	RES MF 249 1% 1/4W	0104-24900	74902
2	R10,R11	RES MF 442 1% 1/4W	0104-44200	74902
2	R31,R32	RES MF 499 .1% 1/4W	0105-49900	74902
2	R35,R36	RES MF 750 1% 1/4W	0104-75100	74902
2	R2,R7	RES MF 825 1% 1/4W	0104-82500	74902
19	R63,R64,R66-79, R104-105,R119	RES MF 1K 1% 1/4W	0104-10010	74902
1	R92	RES MF 1.15K 1/4W 1%	0104-11510	74902
1	R73	RES MF 1.33K .1% 1/4W	0105-13310	74902
2	R86,R87	RES MF 1.5K 1/2W 1%	0104-1501A	74902
2	R3,R20	RES MF 2K 1% 1/4W	0104-20010	74902
2	R22,R24	RES MF 2.49K 1% 1/4W	0104-24910	74902
1	R88	RES MF 6.34K 1% 1/2W	0104-6341A	74902
4	R23,R69,R97,R98	RES MF 10K 1% 1/4W	0104-10020	74902
1	R38	RES MF 20K 1% 1/4W	0104-20020	74902
2	R82,R83	RES MF 24K .1% 1/4W	0105-24020	74902
1	R84	RES VAR 100R 3386 W	0203-0101A	80294
1	R91	RES VAR 200 3386W-1-201	0203-0201A	80294
2	R95	RES VAR 2K3386W	0203-0202A	80294
1	RN1	RES NET MSP-05-01-33G 33K/5	0110-0333B	91637
1	U1	ANALOG SWITCH SD5000N	0500-57110	17856
1	U2	DAC AD834	0500-60100	24355
1	U3	QUAD COMP LM339N	0500-50400	04713
3	U4,U11,U13	8 BIT SHIFT REGISTER CD4094B	0540-01100	27014
1	U5	DUAL OP AMP LM1458N	0500-56500	04713
1	U6	TRIPLE LINE REC 10216	0500-41100	04713
1	U7	SINGLE OP AMP TL081CP	0500-56700	04713
1	U8	OP AMP LM 741C	0500-56310	04713
1	U9	HIGH FREQ OP AMP CLC404AJP	0560-00300	62839
1	U10	D/A 10 BIT CONVERTER AD7533JN	0560-00700	1ES66
1	U12	BUFFER 9668 (L204)	0500-11600	04713
2	U14,U15	SUPER GAIN OP AMP OP07CP	0500-56330	04713
1	U16	OP AMP LM393N	0500-53700	04713
1	U17	ANALOG SWITCH NE521N	0500-54500	18324
	Pulse Generator Board Assembly		***6100-6250***	***23338***
1	C34	CAP POLY 0.01µ 63V 2222.371.12103	1522-01030	59821
1	C3	CAP POLY 47n 63V 2222.371.22473	1522-04730	59821
1	C2	CAP POLY 470n 63V 2222.371.12474	1522-04740	59821
1	C1	CAP POLY 4.7µ 63V 2222.368.22475	1522-04750	59821
1	C4	CAP POLY 4.7n 63V 2222.371.52472	1522-04720	59821
1	C35	CAP POLY 0.1µ 63V 2222.371.12104	1522-01040	59821
1	C32	CAP POLY 1µ 100V 2222.344.21105	1522-0105A	59821

Table 8-2. Model 8551 - Parts List (continued)

Qty	Reference Designation	Description and Commercial Part Number	Tabor Part Number	Vendor Code
4	C5-C8	CAP ELEC 100µ 25V 2222.036	1533-01070	59821
1	C36	CAP ELEC 100µ 16V 2222.013	1532-0107P	59821
1	C10	CAP CER 22P SR155C220MAA	1500-02200	96095
1	C23	CAP CER 33P SR155C330MAA	1500-03300	96095
1	C9	CAP CER 430P SR155C431MAA	1500-04310	96095
5	C17,C18,C30,C39,C44	CAP CER 1n SR155C102MAA	1500-01020	96095
3	C11,C15,C31	CAP CER 0.1µ SR155C104ZAA	1500-01040	96095
8	C14 C19-C20,C24-26, C40-41	CAP CHIP 0.1µ C0805A104Z5AC	1560-01040	31433
8	C12 C13 C16 C21, C37-38,C42-43	CAP TANT 10µ T350B106M025AS	1540-0106B	31433
1	C27	CAP CER 10n SR155C103MAA	1500-01030	96095
1	C33	CAP MICA 910P CD15ED911J03	1510-09110	14665
3	CR1,CR2,CR7	DIODE ZENER 1N746A 3.3V	0300-20000	14936
2	CR4,CR6	DIODE ZENER 1N747A 3.6V	0300-20110	14936
2	CR3,CR5	DIODE ZENER 1N753A 6.2V	0300-20200	14936
2	K1,K3	RELAY DIP 1A 5V HE721A-0100	0900-01100	12617
1	K2	RELAY DIP 1C 5V HE721C-0100	0900-01000	12617
21	Q2-7,Q13,Q15,Q16, Q19,Q20,Q26,Q27, Q29-34,Q36,Q37	TSTR PN3904	0400-01200	04713
6	Q1,Q14,Q17,Q18, Q21,Q38	TSTR PN3906	0400-01340	04713
4	Q9,Q10,Q22,Q24	TSTR MPS3640	0400-00100	04713
2	Q11,Q12	TSTR BFY-90	0400-00710	04713
3	Q23,Q25,Q35	TSTR 2N5179	0400-00700	04713
2	Q28,Q39	TSTR J-309	0400-02510	17856
1	Q8	TSTR 2N5912	0400-40500	17856
2	R30,R32	RES COMP 22 5% 1/4W	0100-02200	74902
1	R78	RES COMP 22 5% 1/8W BB2205	0102-02200	74902
2	R81,R94	RES COMP 33 5% 1/4W	0100-03300	74902
2	R48,R49	RES COMP 47 5% 1/4W	0100-04700	74902
1	R77	RES COMP 82 5% 1/4W	0100-08200	74902
2	R23,R79	RES COMP 100 5% 1/4W	0100-01010	74902
1	R74	RES COMP 130 5% 1/4W	0100-01310	74902
1	R60	RES COMP 300 5% 1/4W	0100-03010	74902
5	R27,R52,R53,R59,R63	RES COMP 510 5% 1/4W	0100-05110	74902
4	R57,R61,R82,R93	RES COMP 560 5% 1/4W	0100-05610	74902
4	R3,R4,R73,R86	RES COMP 1K 5% 1/4W	0100-01020	74902
9	R6,R15-18,R20,R31, R33,R55	RES COMP 2.2K 5% 1/4W	0100-02220	74902
2	R54,R69	RES COMP 2.7K 5% 1/4W	0100-02720	74902
2	R56,R58	RES COMP 3.3K 5% 1/4W	0100-03320	74902

Table 8-2. Model 8551 - Parts List (continued)

Qty	Reference Designation	Description and Commercial Part Number	Tabor Part Number	Vendor Code
1	R26	RES COMP 4.7K 5% 1/4W	0100-04720	74902
6	R1,R2,R19,R95,R97,R62	RES COMP 10K 5% 1/4W	0100-01030	74902
1	R92	RES COMP 1M 5% 1/4W	0100-01050	74902
2	R71,R85	RES MF 10 1% 1/4W	0104-10R00	74902
2	R72,R80	RES MF 33.2 1% 1/4W	0104-33R20	74902
2	R28,R29	RES MF 49.9 1% 1/4W	0104-49R90	74902
1	R25	RES MF 61.9 1% 1/4W	0104-61R90	74902
4	R34,R36,R67,R70	RES MF 100 1% 1/4W	0104-10000	74902
2	R38,R40	RES MF 200 1% 1/4W	0104-20000	74902
1	R83	RES MF 402 1% 1/4W	0104-40200	74902
6	R35,R37,R39,R41, R42,R44	RES MF 499 1% 1/4W	0104-49900	74902
2	R50,R51	RES MF 619 1% 1/4W	0104-61900	74902
1	R12	RES MF 1K 1% 1/4W	0104-10010	74902
4	R43,R45,R87,R88	RES MF 1.1K 1% 1/4W	0104-11010	74902
1	R89	RES MF 1.24K 1% 1/4W	0104-12410	74902
2	R46,R47	RES MF 1.5K 1/4W 1%	0104-15010	74902
5	R64,R65,R75,R84,R96	RES MF 4.99K 1% 1/4W	0104-49910	74902
8	R5,R7,R10,R11,R90, R91,R98,R104	RES MF 10K 1% 1/4W	0104-10020	74902
1	R76	RES MF 20K 1% 1/4W	0104-20020	74902
1	R9	RES MF 23.2K 1% 1/4W	0104-23220	74902
1	R8	RES MF 33.2K 1% 1/4W	0104-33220	74902
2	R13,R21	RES MF 100K 1% 1/4W	0104-10030	74902
1	R101	RES MF 249K 1% 1/4W	0104-24930	74902
1	R103	RES MF 301K 1% 1/4W	0104-30130	74902
2	R14,R68	RES MF 332K 1% 1/4W	0104-33230	74902
2	R99,R102	RES MF 2M 1% 1/4W	0104-20040	74902
1	R66	RES VAR 20K 3386W-1-203	0203-0203A	80294
1	R100	RES VAR 250K 3386W-1-254	0203-0254A	80294
1	RN1	RES NET MSP-08A-03-182G 1.8K/8	0110-01820	91637
1	RN2	RES NET MSP-05-01-272G 2.7K/5	0110-0272B	91637
1	RN3	RES NET MDP-14-03-222G 2.2K/14	0108-02220	91637
2	U1,U22	DUAL OP AMP LM1458N	0500-56500	04713
1	U2	OP AMP OP200GP	0500-56350	24355
7	U4,U9,U12,U13,U14, U26,U28	8 BIT SHIFT REGISTER CD4094B	0540-01100	27014
1	U5	HA3-5033-5	0500-56340	36472
2	U6,U7	OP AMP OP400GP	0500-56370	24355
3	U8,U11,U24	D/A 10 BIT CONVERTER AD7533JN	0560-00700	1ES66
2	U10,U16	ECL NOR MC10102P	0500-40900	04713
3	U3,U15,U17	QUAD OP AMP LM324N	0500-53210	04713
1	U18	ECL FLIP-FLOP MC10H131P	0500-45300	04713
2	U19,U21	OP AMP TL081CP	0500-56700	04713

Table 8-2. Model 8551 - Parts List (continued)

Qty	Reference Designation	Description and Commercial Part Number	Tabor Part Number	Vendor Code
1	U20	COMPARATOR MAX9690CPA	0500-60950	1ES66
1	U23	OP AMP LM 741C	0500-56310	04713
1	U25	ANALOG SWITCH DG411CJ	0500-91000	17856
1	U27	DUAL OP AMP TL082CP	0500-56600	04713
CPU Board Assembly			***6100-6200***	***23338***
13	C1-2,C4-14	CAP CER 0.1µ SR155C104ZAA	1500-01040	96095
1	C3	CAP TANT 3.3µ T350A335M025AS	1540-03350	31433
1	C15	CAP ELECTR 470µ 25V 2222.037	1533-04770	59821
2	J1,J2	CON FEMALE 2X8 90152-2216	3000-30520	27264
1	J3	CON MALE 2X10 90131-0770	3000-30260	27264
1	J4	CON MALE 2X13 90131-0773	3000-30290	27264
1	Q1	TSTR PN3904	0400-01200	04713
1	Q2	TSTR 2N4401	0400-01810	04713
1	R1	RES COMP 3.3K 5% 1/4W	0100-03320	74902
3	R2,R3,R4	RES COMP 1K 5% 1/4W	0100-01020	74902
2	R5,R6	RES COMP 510 5% 1/4W	0100-05110	74902
1	RN1	RES NET MDP-16-03-150G 15/16	0109-01500	91637
1	U1	BUFFER ULN2004N	0500-11600	04713
1	U2	KEYBOARD/DISPLY P8279	0500-20700	34639
1	U3	IC 74LS138	0510-02700	04713
1	U4	HEX INVERTER 74HC4049	0520-07300	04713
1	U5	CONTROLLER P8031	0500-21410	34639
1	U6	COUNTER/DIVIDER 74HC4040	0520-07000	04713
1	U7	LOW POWER SCHOTTKEY 74LS373	0510-03650	04713
1	U8	EPROM 27C512	0500-21250	23338
1	U9	RAM MK48ZO2B-200PSI	0500-11160	66958
1	U10	32BIT BINARY COUNTER LS7062	0550-00300	55261
1	U12	IC 74LS02	0510-00110	04713
1	U13	IC 74LS00	0510-00100	04713
1	U14	IC 74F74	0500-12600	04713
1	U15	GPIB CONTROLLER P8291A	0500-21300	34639
1	U16	GPIB BUFFER DS75161N	0500-21520	27014
1	U17	GPIB BUFFER DS75160N	0500-21510	27014
1	Y1	CRYSTAL 10MHz CY-12A	0800-30000	75378
VCO Board Assembly			***6100-6220***	***23338***
1	C46	CAP CER 27P SR155C270KAA	1500-02700	96095
1	C36	CAP CER 33P SR155C330KAA	1500-03300	96095
1	C16	CAP CER 100P SR155C100KAA	1500-01010	96095
1	C39	CAP CER 1n SR155C102KAA	1500-01020	96095

Table 8-2. Model 8551 - Parts List (continued)

Qty	Reference Designation	Description and Commercial Part Number	Tabor Part Number	Vendor Code
4	C27,C47,C48,C49	CAP CER 10n SR155C103KAA	1500-01030	96095
17	C13-14,C17-20,C28-29, C32-33,C37-38,C40,C42, C43-45	CAP CHIP 0.1µ C0805A104Z5AC	1560-01040	31433
1	C15	CAP CER 0.1µ SR155C104ZAA	1500-01040	96095
1	C23	CAP POLY 4.7n 63V 2222.371.52472	1522-04720	59821
1	C22	CAP POLY 47n 63V 2222.371.22473	1522-04730	59821
1	C21	CAP POLY 0.47µ 63V 2222.371.12474	1522-04740	59821
1	C50	CAP MYL 1µ 100V 2222.344.21105	1522-0105A	59821
1	C24	CAP MICA 430P CD15ED431J03	1510-04310	14655
6	C1,C2,C3,C4,C5,C6	CAP ELEC 100µ 25V 2222.036	1533-01070	59821
6	C7,C10,C26,C34,C35,C51	CAP TANT 10µ T350B106M025AS	1540-0106B	31433
3	CR1,CR3,CR5	DIODE 1N4151	0300-00400	14936
2	CR8,CR9	DIODE ZENER 1N749A - SELECTED	0300-20900	23338
2	CR11,CR12	DIODE 1N753A 6.2V MATCHED	0300-20200	23338
1	CR2	DIODE ZENER 1N759A 12V	0300-20500	14936
1	CR4	DIODE ZENER 1N756A 8.2V	0300-20700	14936
2	CR6,CR7	DIODE ZENER 1N746A	0300-20000	14936
2	CR10,CR13	DIODE HOT CARRIER 5082-2835	0300-10300	54893
2	J1,J2	CON FEMALE 2X8 90152-2216	3000-30520	27264
2	J3,J4	CON RF MALE 131-1701-201	3000-16000	74970
1	K1	RELAY RY-05WK-R10	0900-00700	55101
1	K2	RELAY DIP 1A 5V HE721A-0100	0900-01100	12617
1	K3	RELAY DIP 2A 5V HE722A-0100	0900-01200	12617
4	L1-L4	BEAD Ferrite CERAMAG24 57-1355	4200-00000	59821
1	Q1	TSTR J-109	0400-02500	17856
1	Q12	TSTR J-309	0400-02510	17856
7	Q8-11,Q16,Q21,Q27	TSTR PN3904	0400-01200	04713
4	Q15,Q17,Q18,Q33	TSTR PN3906	0400-01340	04713
8	Q4,Q6,Q7,Q23,Q24,Q25, Q31,Q32	TSTR MPS3640	0400-00100	04713
4	Q2,Q3,Q5,Q28	TSTR MPS3646	0400-00200	04713
4	Q13,Q14,Q19,Q20	TSTR 2N3960	0400-20000	04713
		TSTR PN5771	0400-00750	04713
1	Q22	TSTR PN5087	0400-01900	04713
3	Q26,Q29,Q30	TSTR 2N5179	0400-00700	04713
2	R43,R44	RES COMP 10 5% 1/8W BB1005	0102-01000	74902
4	R36,R86,R88,R89	RES COMP 22 5% 1/8W BB2205	0102-02200	74902
13	R29-32,R35,R38,R40, R53,R57,R66,R68, R75,R84	RES COMP 33 5% 1/8W BB3305	0102-03300	74902
2	R46,R72	RES COMP 33 5% 1/4W	0100-03300	74902
1	R27	RES COMP 39 5% 1/8W BB3905	0102-03900	74902

Table 8-2. Model 8551 - Parts List (continued)

Qty	Reference Designation	Description and Commercial Part Number	Tabor Part Number	Vendor Code
1	R132	RES COMP 47 5% 1/4W	0100-04700	74902
1	R28	RES COMP 51 5% 1/8W	0102-05100	74902
1	R137	RES COMP 82 5% 1/4W	0100-08200	74902
7	R52,R73,R74,R87,R93, R94,R118	RES COMP 100 5% 1/8W BB1015	0102-01010	74902
6	R85,R102,R105,R120, R133,R134	RES COMP 100 5% 1/4W	0100-01010	74902
1	R138	RES COMP 130 5% 1/4W	0100-01310	74902
1	R136	RES COMP 220 5% 1/4W	0100-02210	74902
9	R14,R15,R56,R60,R61, R65,R67,R108,R109	RES COMP 270 5% 1/8W BB2715	0102-02710	74902
1	R104	RES COMP 300 5% 1/4W	0100-03010	74902
1	R82	RES COMP 510 1/8W 5%	01020-0511	74902
12	R110,R111,R113,R116, R117,R122-124,R126, R128-130	RES COMP 560 1/8W 5%	0102-05610	74902
4	R47,R48,R49,R50	RES COMP 1K 5% 1/4W	0100-01020	74902
1	R83	RES COMP 1.5K 5% 1/4W	0100-01520	74902
2	R106,R107	RES COMP 1.8K 1/8W 5%	0102-01820	74902
1	R140	RES COMP 1.8K 5% 1/4W	0100-01820	74902
1	R114	RES COMP 2K 5% 1/4W	0100-02020	74902
2	R103,R119	RES COMP 2.2K 5% 1/4W	0100-02220	74902
1	R148	RES COMP 2.7K 5% 1/4W	0100-02720	74902
2	R9,R10	RES COMP 3.3K 5% 1/4W	0100-03320	74902
1	R143	RES COMP 10K 5% 1/4W	0100-01030	74902
2	R11,R13	RES COMP 33K 5% 1/4W	0100-03330	74902
3	R23 R24 R135	RES MF 49.9 1% 1/4W	0104-49R90	74902
1	R51	RES MF 61.9 1% 1/8W	0102-61R9A	74902
1	R76	RES MF 100 1% 1/4W	0104-10000	74902
2	R54 R55	RES MF 115 1% 1/8W	0102-1150A	74902
2	R58 R59	RES MF 127 1%1 1/8W	0102-1270A	74902
2	R62 R63	RES MF 140 1% 1/8W	0102-1400A	74902
2	R70 R71	RES MF 154 1% 1/8W	0102-1540A	74902
1	R77	RES MF 200 1% 1/4W	0104-20000	74902
3	R12 R98 R100	RES MF 249 1% 1/4W	0104-24900	74902
2	R64 R69	RES MF 261 1% 1/8W	0102-2610A	74902
4	R41 R42 R115 R127	RES MF 330 1% 1/8W	0102-03310	74902
1	R131	RES MF 365 1% 1/4W	0104-36500	74902
1	R121	RES MF 464 1% 1/4W	0104-46400	74902
3	R17 R33 R81	RES MF 499 1% 1/8W	0102-4990A	74902
1	R37	RES MF 619 1% 1/8W	0102-6190A	74902
2	R90 R91	RES MF 820 1% 1/8W	0102-08210	74902
1	R18	RES MF 825 1% 1/8W	0102-8250A	74902
2	R5 R16	RES MF 1K 1% 1/4W	0104-10010	74902
3	R45,R112,R139	RES MF 1K 1% 1/8W	0102-01020	74902
3	R96,R97,R99	RES MF 1K 0.1% 1/4W	0105-10010	74902

Table 8-2. Model 8551 - Parts List (continued)

Qty	Reference Designation	Description and Commercial Part Number	Tabor Part Number	Vendor Code
1	R8	RES MF 1.1K 1% 1/4W	0104-11010	74902
1	R19	RES MF 1.13K 1% 1/8W	0102-1131A	74902
2	R20,R34	RES MF 1.87K 1% 1/8W	0102-1871A	74902
1	R95	RES MF 2 K .1% 1/4W	0105-20010	74902
1	R80	RES MF 2.49K 1% 1/4W	0104-24910	74902
4	R26,R78,R79,R142	RES MF 4.99K 1% 1/4W	0104-49910	74902
1	R7	RES MF 6.81K 1% 1/4W	0104-68110	74902
1	R39	RES MF 7.32K 1% 1/8W	0102-7321A	74902
1	R25	RES MF 9.09K 1% 1/4W	0104-90910	74902
2	R2,R3	RES MF 10K 1% 1/4W	0104-10020	74902
1	R150	RES MF 20K 1% 1/4W	0104-20020	74902
1	R1	RES MF 51.1K 1% 1/4W	0104-51120	74902
2	R4,R141	RES MF 100K 1% 1/4W	0104-10030	74902
1	R6	RES MF 1M 1% 1/4W	0104-10040	74902
2	R92,R144	RES CHIP 5% 33	0113-03300	96095
1	R101	RES VAR 20K 3386W-1-203	0203-0203A	80294
1	R21	RES VAR 2K 3386W-1-202	0203-0202A	80294
1	R22	RES VAR 1K3386W	0203-0102A	80294
1	RN1	5X1K CSC06A-01-102J	0110-1102B	91637
1	U1	OP AMP TL081CP	0500-56700	04713
2	U2,U28	ANALOG SWITCH DG411DJ	0500-91000	17856
3	U3,U17,U18	OP AMP OP07CP	0500-56330	04713
4	U4,U6,U24,U25	8 BIT SHIFT REGISTER CD4094BCN	0540-01100	27014
1	U5	QUAD OP AMP LM324N	0500-53210	04713
1	U7	BUFFER ULN2004N	0500-11600	04713
1	U8	OP AMP LM741C	0500-56310	04713
3	U9,U11,U12	TRANS ARRAY CA3127E	0500-60000	36472
1	U10	HA3-5033-5	0500-56340	36472
1	U13	MAX9690CPA	0500-60950	1ES66
1	U14	DUAL OP AMP TL082CP	0500-56600	04713
1	U15,U29	OP AMP OP 200GP	0500-56350	24355
1	U16	ECL FLIP-FLOP MC10H131P	0500-45300	04713
3	U19,U20,U22	ECL MC10HO16P	0500-45600	04713
1	U21	ECL OR/NOR GATE MC10H105P	0500-45100	04713
2	U23,U27	ECL NOR MC10102P	0500-40900	04713
1	U26	QUAD COMP LM339N	0500-50400	04713

Table 8-2. Model 8551 - Parts List (continued)

Qty	Reference Designation	Description and Commercial Part Number	Tabor Part Number	Vendor Code
Rear Panel Assembly			***6100-6280***	***23338***
1	T1	MAINS TRANSFORMER	2500-05000	23338
1	J1	MAINS RECEPT & FILTER 3EEA1	3000-20500	61935
1	J4	CON GPIB 57FE-2 0240-20ND35	3000-40300	03554
1	S2	SW LINE SELECT EPS1SL1	2000-10220	82389
1	F1	FUSE 1A/250V S/B 5x20 218.001	1100-15600	75915
1	FA1	FAN 12VDC ST-60X12A	1700-00100	62712
Model 8551, List of Assemblies				
		Main Board Assembly	6100-61850	23338
		C.P.U. Board Assembly	6100-62000	23338
		Current Generator Board Assembly	6100-62100	23338
		V.C.O. Board Assembly	6100-62200	23338
		Pulse Generator Board Assembly	6100-62500	23338
		Output Amplifier Board Assembly	6100-62300	23338
		Front Panel Board Assembly	6100-61910	23338
		Rear Panel Assembly	6100-62800	23338
		Case Assembly	6100-62700	23338

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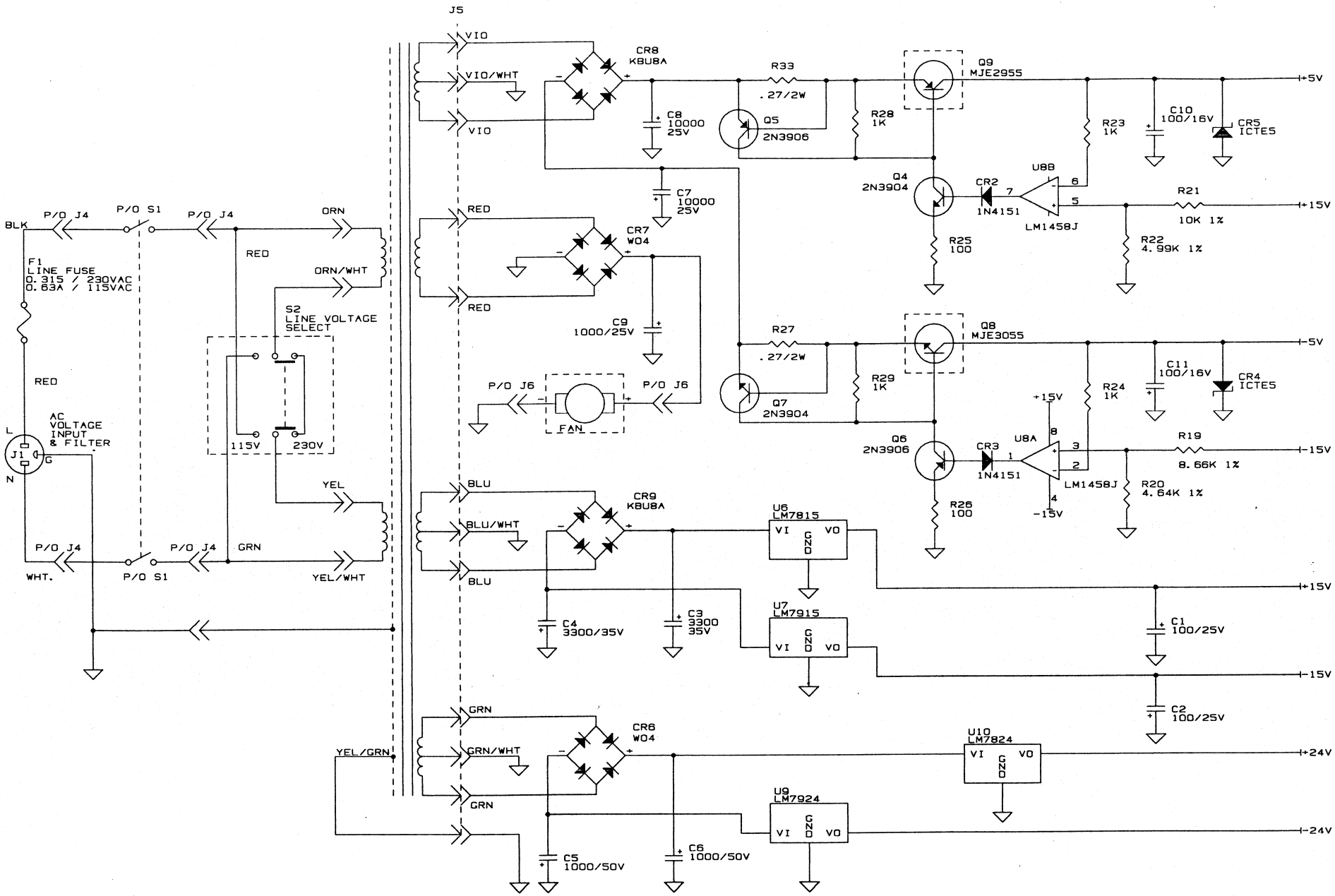

Figure 9-1. Main Board - Power Supply

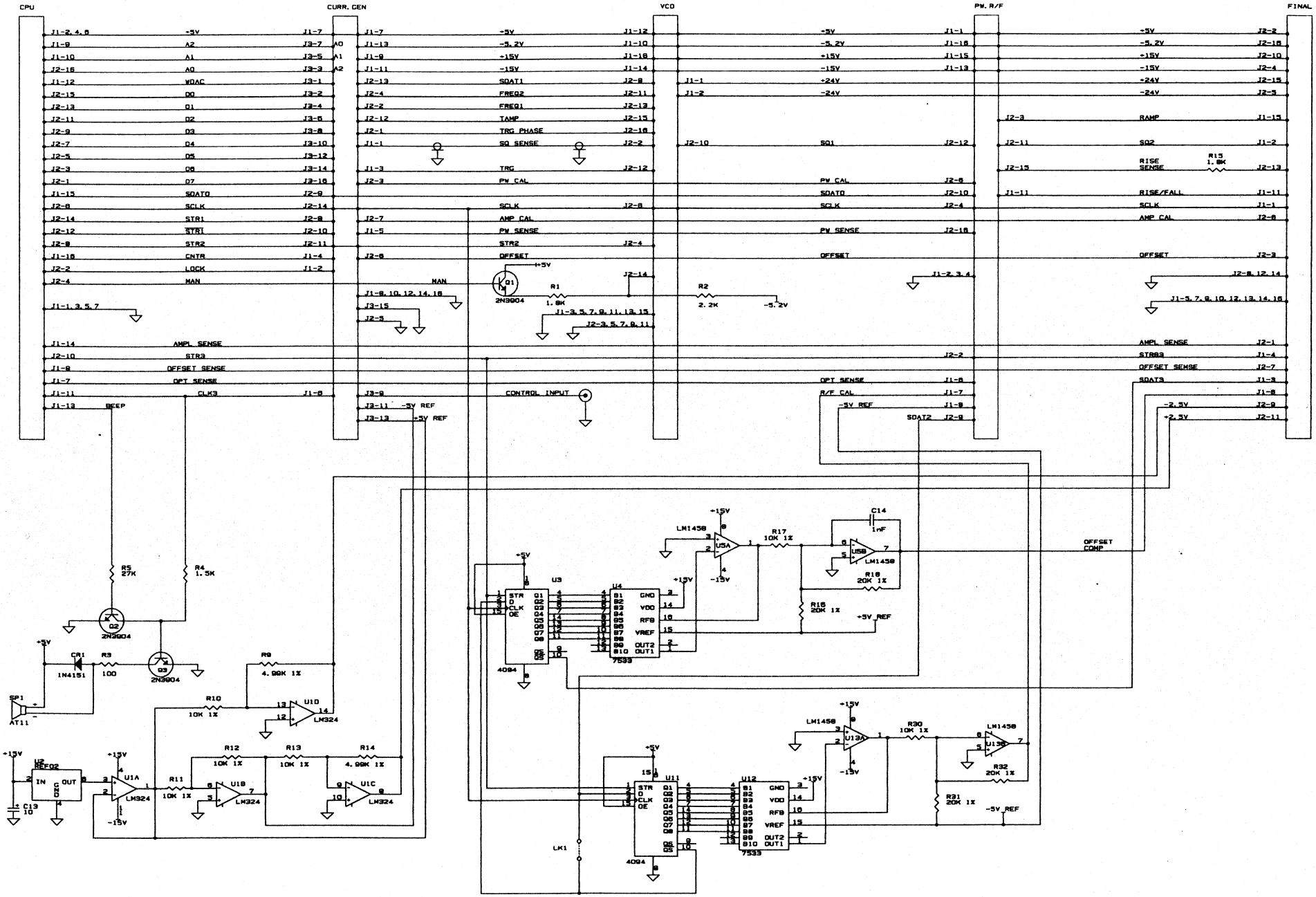

Figure 9-2. Main Board - Inter-connection Diagram

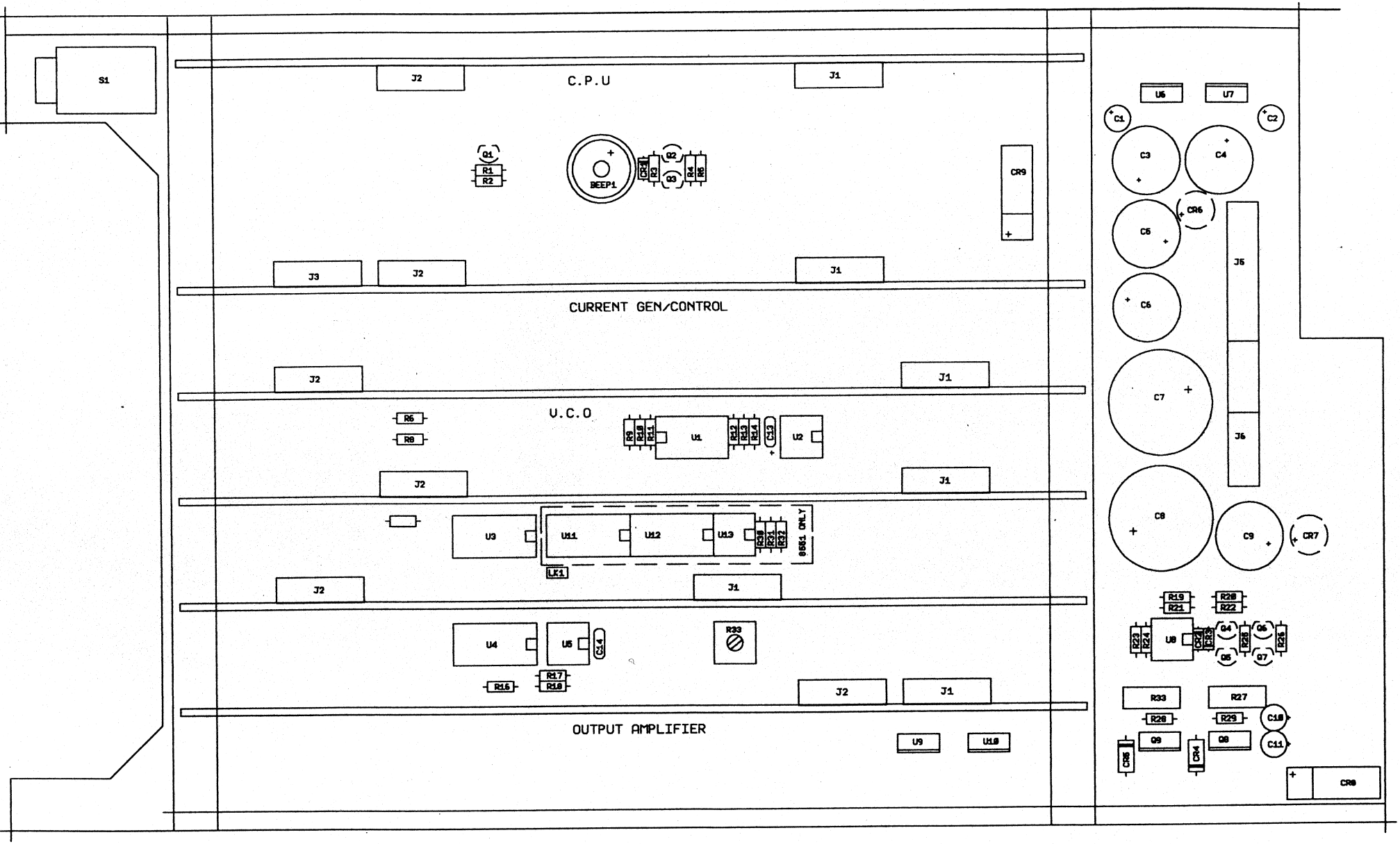

Figure 9-3. Main Board - Components Location

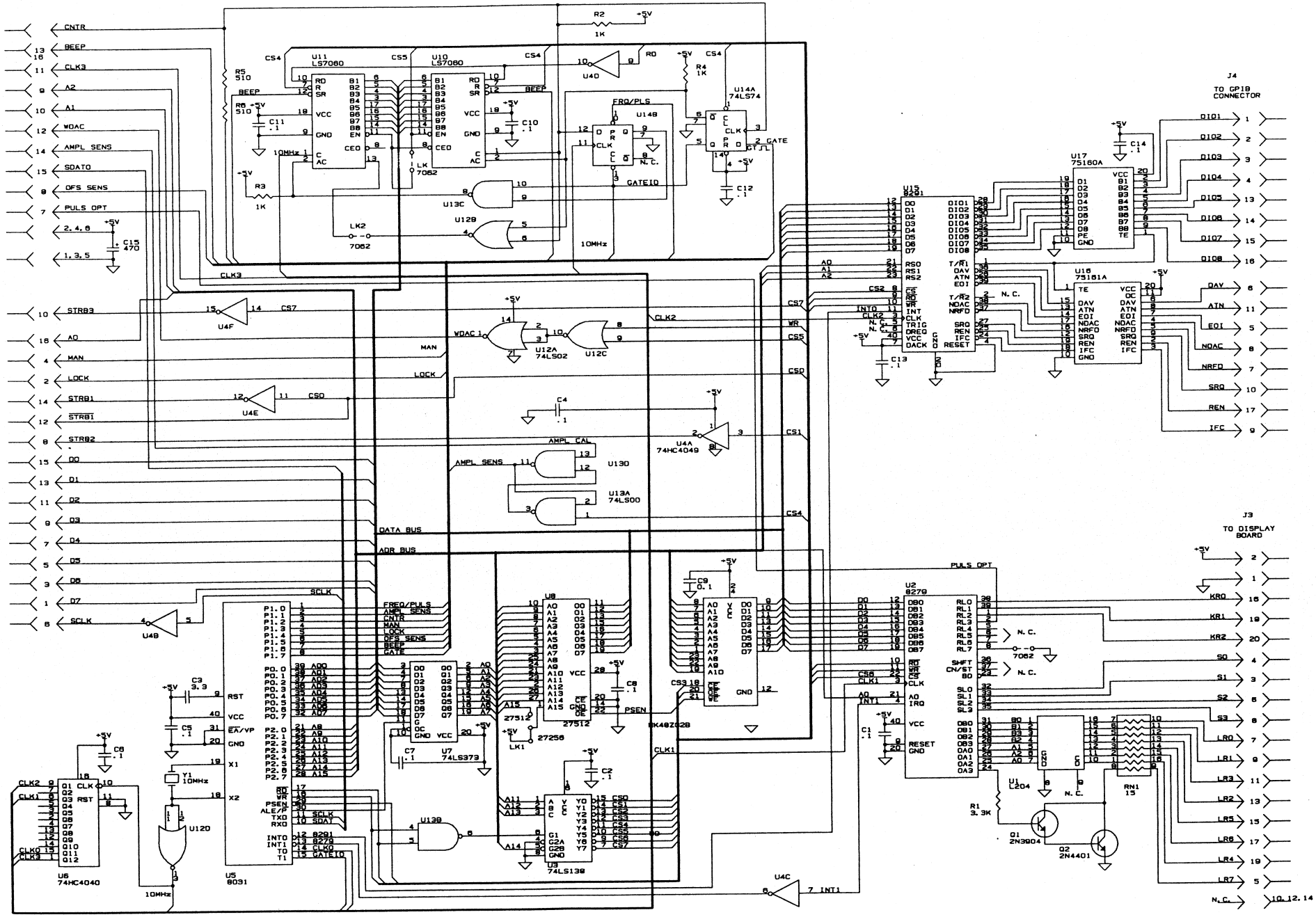

Figure 9-4. CPU Board

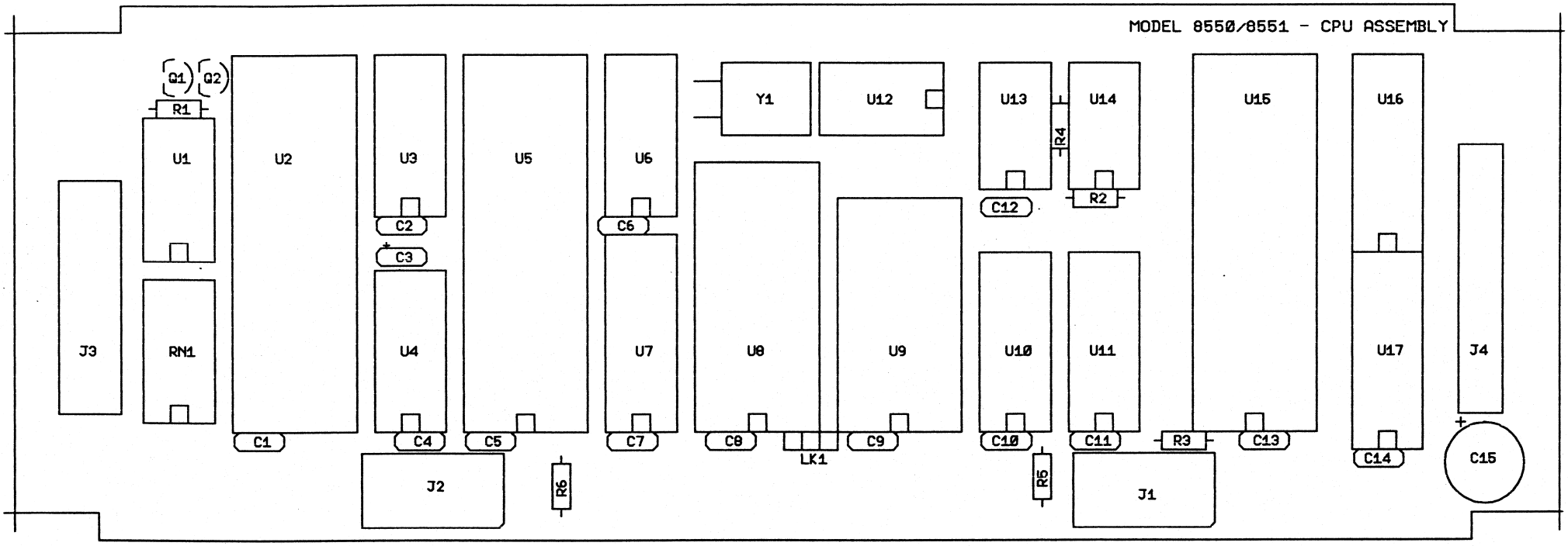

Figure 9-5. CPU Board - Components Location

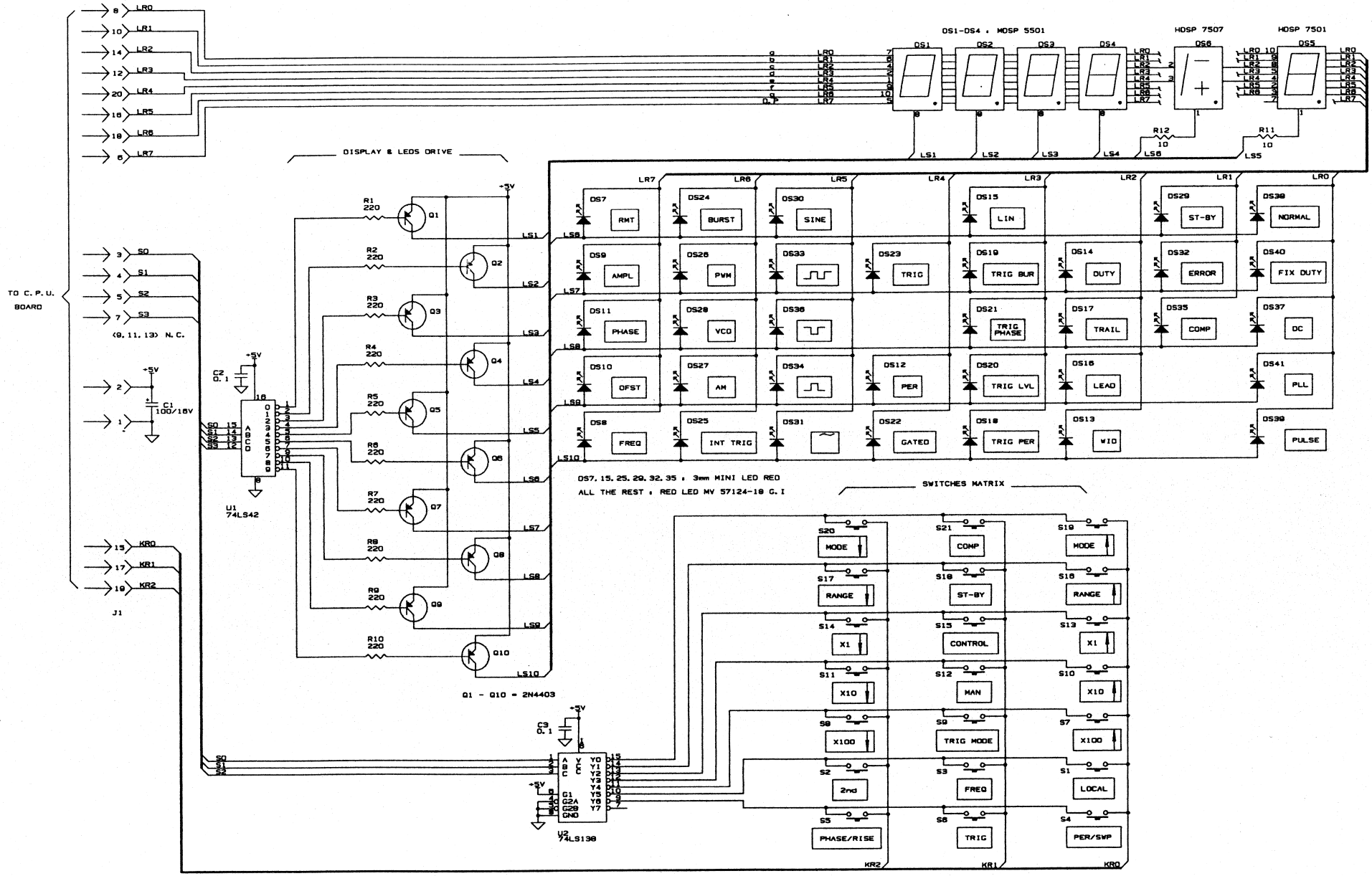

Figure 9-6. Keyboard and Display

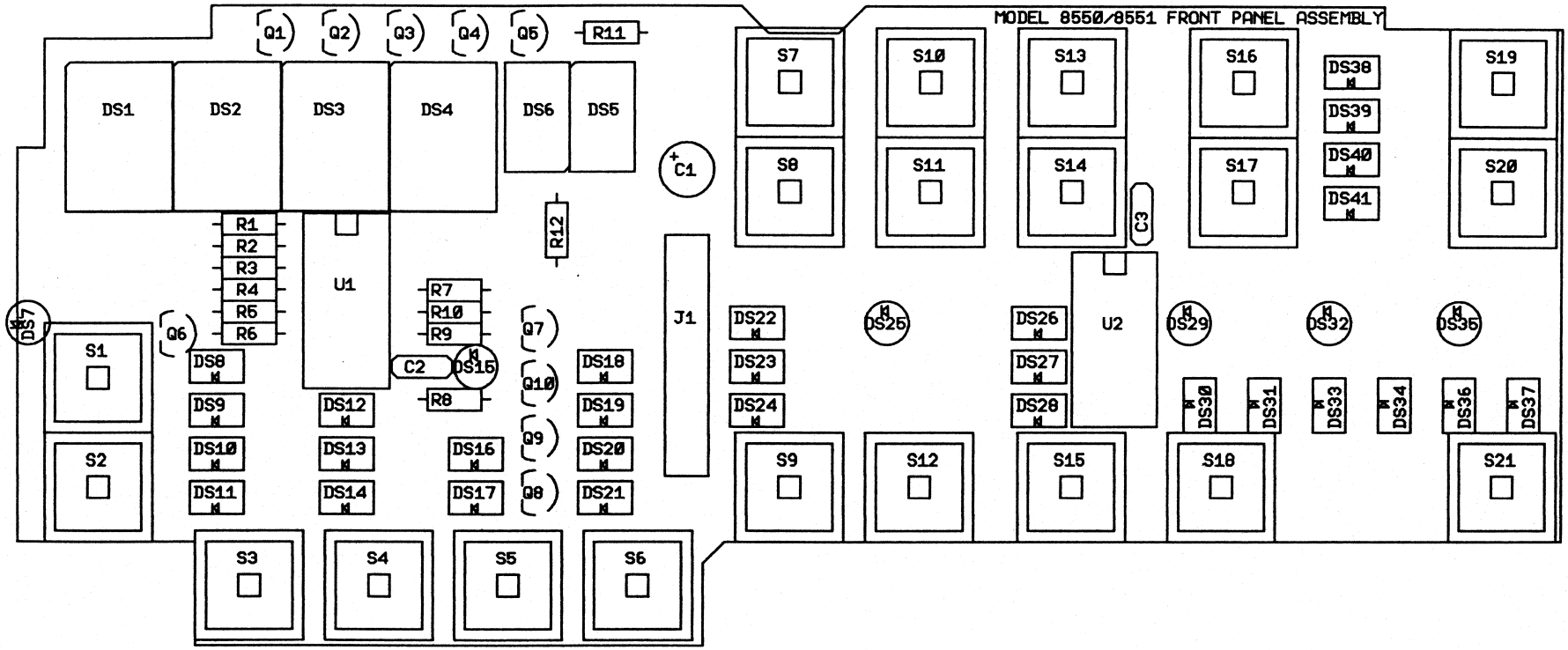

Figure 9-7. Keyboard and Display - Components Location

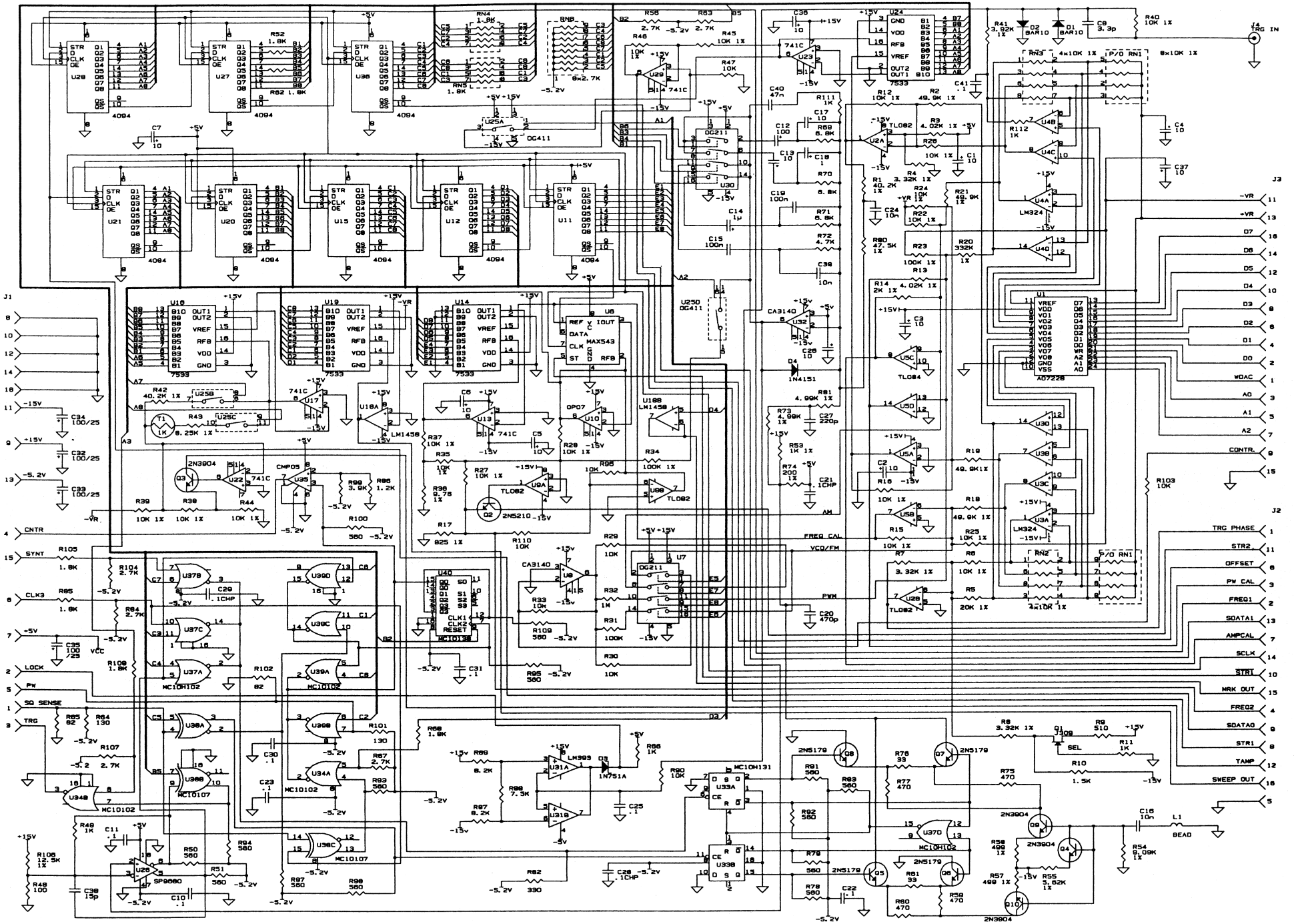

Figure 9-8. Current Generator Board

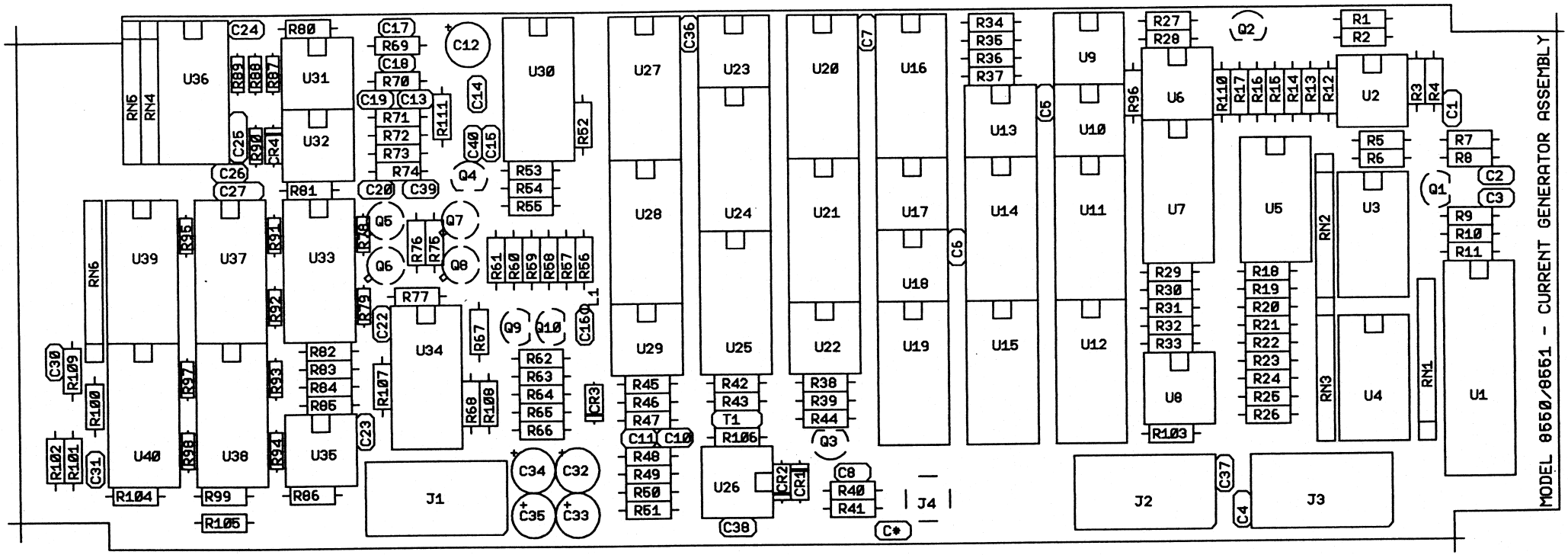

Figure 9-9. Current Generator Board - Components Locati

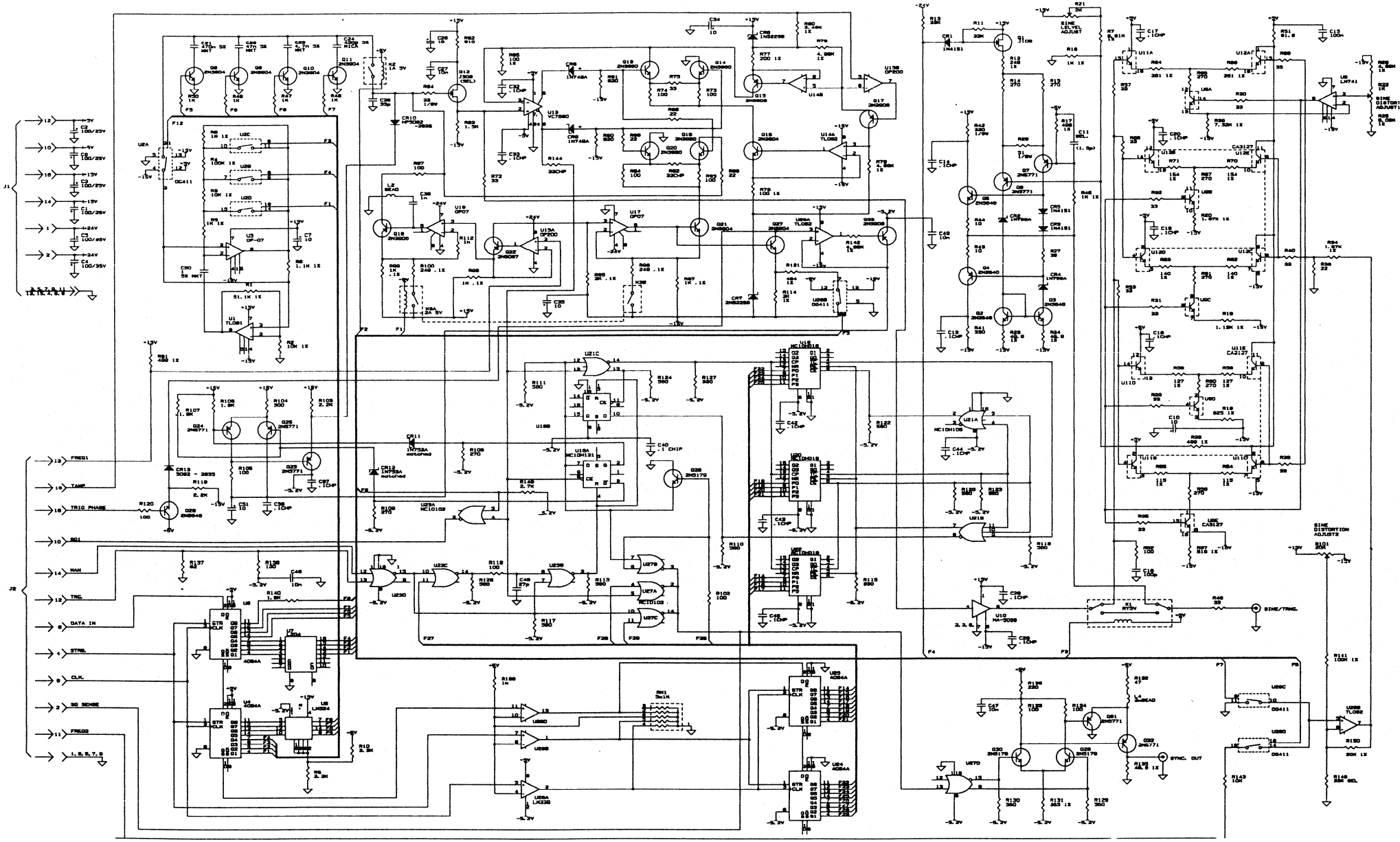

Figure 9-10. VCO Board

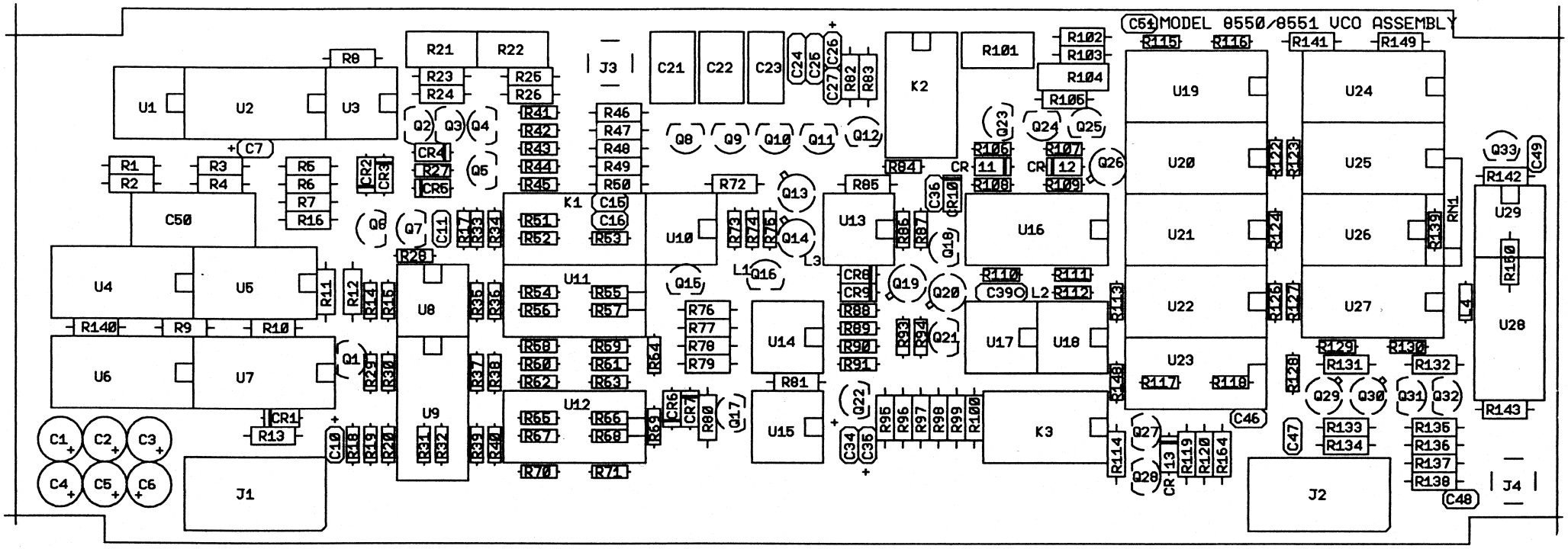

Figure 9-11. VCO Board - Components Location

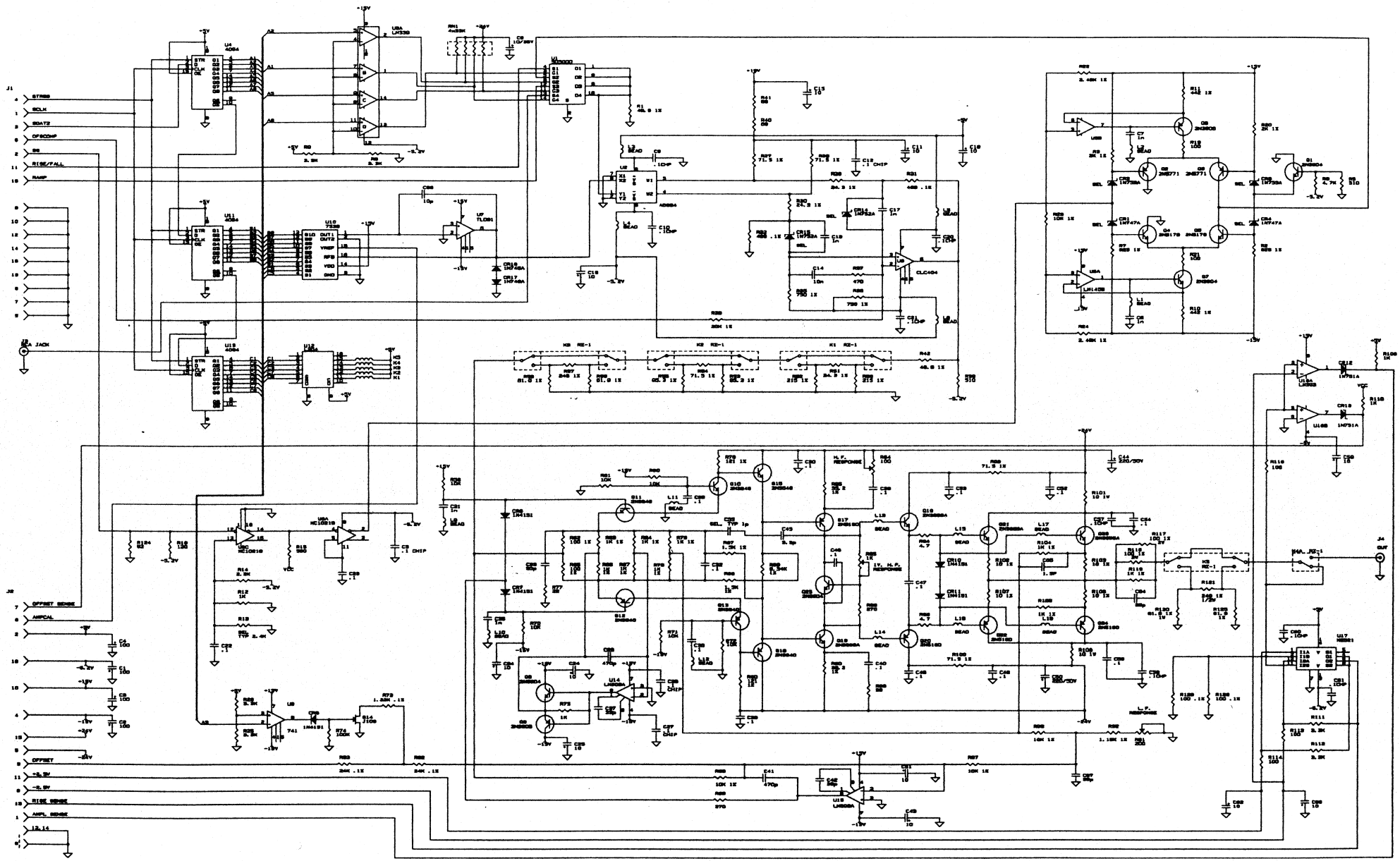

Figure 9-12. Output Amplifier Board

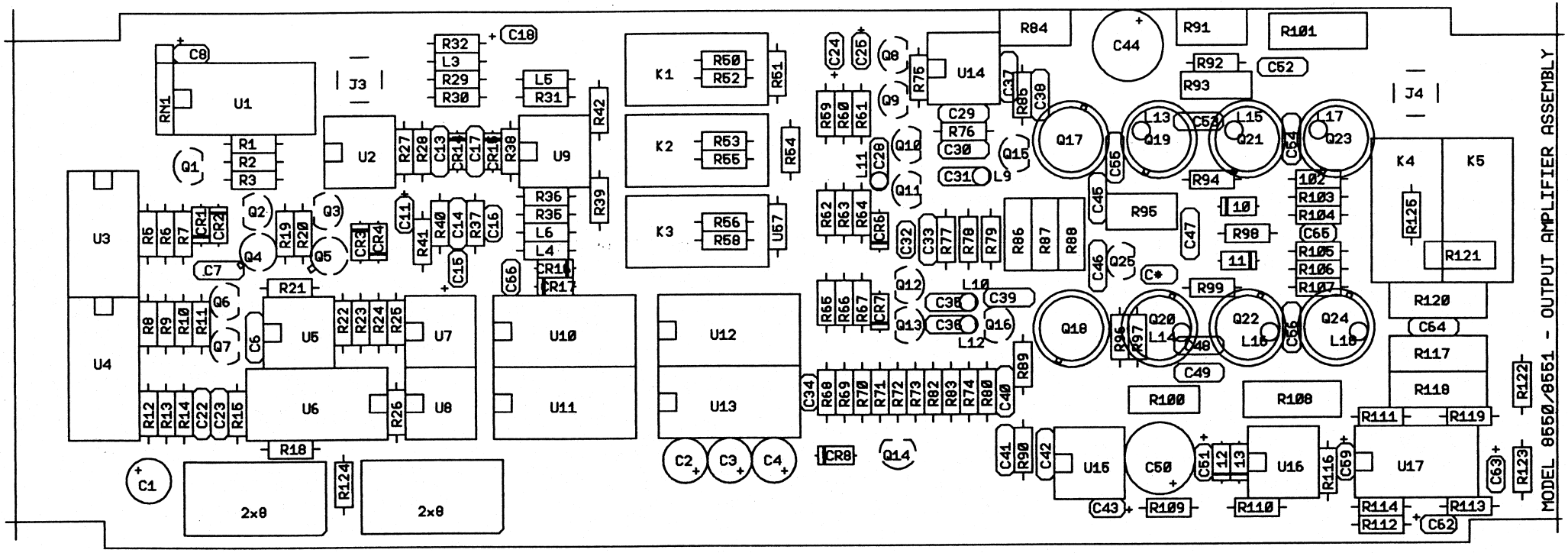

Figure 9-13. Output Amplifier Board - Components Locatic

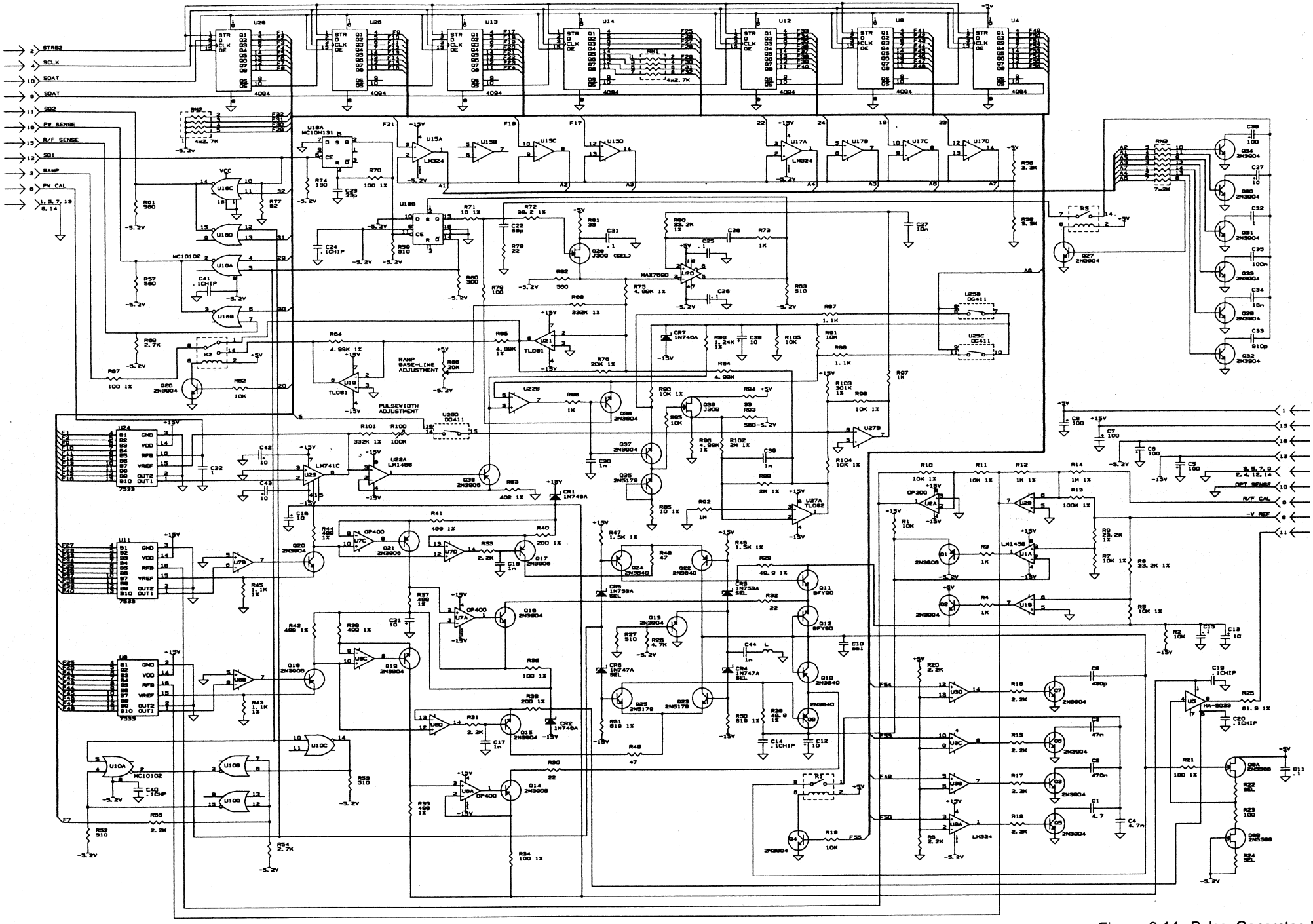

Figure 9-14. Pulse Generator Board

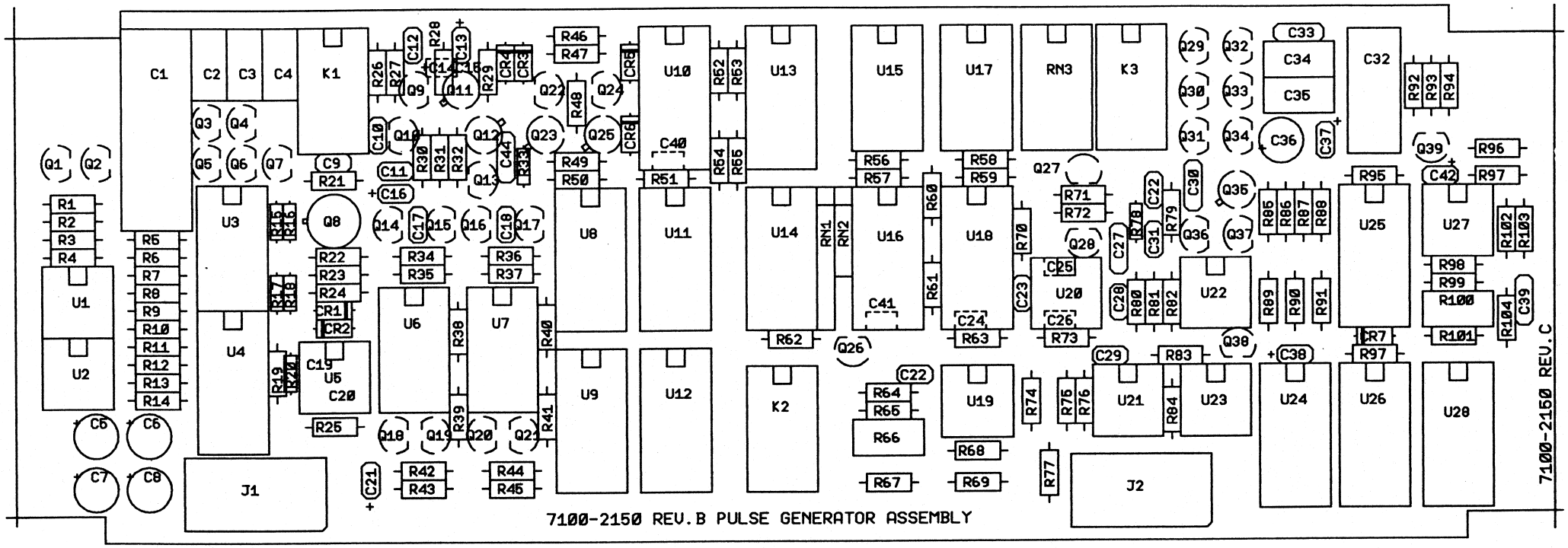

Figure 9-15. Pulse Generator Board - Components Locatic